Analysis and Design of RF CMOS Attenuators

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***Abstract*—Attenuators are analyzed for their minimum Insertion Loss (IL), maximum attenuation and source-load matching performance. These results are used to make trade-offs in the design of a CMOS attenuator with wide dynamic range, designed and fabricated in a 0.13 μm CMOS process. The design employs two non-identical cascaded T-stages that are activated consecutively to improve linearity. The design operates in the frequency band of DC-2.5GHz with 0.9–3.5 dB insertion loss and 42 dB maximum attenuation in the entire frequency range. Worst case S11 is −8.2 dB across the frequency band. The design achieves an IIP3 of +20 dBm at mid-attenuation.**

***Index Terms*—Attenuator, attenuator analysis, attenuation control loop, CMOS attenuator, highly linear attenuator, parasitic effects on attenuators, RF attenuator.**

I. Introduction

THE received signal power in cable and wireless communication systems may vary by orders of magnitude. These systems thus require precise gain control in the signal path to limit the incident power to the receiver circuitry. Similarly, emerging communication standards such as WCDMA require stringent power control on the transmitted signal.

Variable-gain amplifiers (VGAs) are the traditional method of implementing gain control. However, it has been shown in the literature that FET attenuators are also good candidates for achieving the same function with superior performance in various design criteria such as linearity and power handling requirements, which are exteremely important for wideband applications such as cable modem receivers [1]–[3], [6], [18]. These requirements generally are very difficult to meet with VGAs, hence, power dissipation in these components may be hundreds of milliwatts in order to meet these specifications. Attenuators with FET devices in their resistive linear region, on the other hand, are passive blocks and do not dissipate any static power. Furthermore, the downscaling of CMOS technology provides faster devices, which are suitable for broadband RF applications that can be integrated on a single chip. In this work, the design of wideband, highly-linear CMOS attenuators is discussed. The design of a sample attenuator along with the simulated and measured results is given. The attenuator exhibits a linear-in-dB attenuation curve and matches to the port impedances at the input and output over the entire frequency range of operation.

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II. Attenuator Design Analysis

In this section, we analyze different types of attenuators in terms of their design parameters, which are insertion loss (IL), maximum attenuation, source and load matching properties. We will limit our analysis to most commonly used attenuator types, Π-Attenuators and T-Attenuators. Fig. 1 shows the topology of these two configurations.

A. Minimum Insertion Loss

Fig. 2 gives the schematic for the minimum IL condition of a single-stage Π-Attenuator. In a Π-Attenuator such as this one, minimum attenuation occurs when the series device is completely on and the shunt devices are off. In that case, loss at low frequencies comes only from the nonzero on-resistance of the series device. As this resistor gets smaller, the signal loss due to the insertion of the attenuator gets smaller. At higher frequencies, there is additional loss caused by the parasitic capacitors to ground and minimizing these capacitors reduces the loss. Furthermore, for high impedance systems, the finite shunt device off-resistance becomes comparable with the source resistance and causes the series device not to turn on completely in order for good matching, therefore increases the insertion loss.

The parasitic capacitors are mainly due to the gate capacitors of the devices and the junction capacitors between the drain and source implants and the p-substrate of the chip. The gate capacitors consist of the gate-oxide capacitors and the overlap capacitors due to the overlap of the gate area and the source or drain areas. The $R_{\rm Large}$ resistor is placed in series with the gate in order to isolate the gate capacitors, thus minimizing the total parasitic capacitance to ground at a given node and broadbanding the network. Fig. 2 also gives the equivalent lumped resistor-capacitor network for the schematic given in the same figure.

Assuming that the attenuator is symmetric with respect to the input and output nodes, C_{T1} and C_{T2} capacitors are equal in value. These capacitors consist of the gate-oxide and junction parasitic capacitors of the devices as explained above and can be expressed as

$$C_T = C_{T1} = C_{T2} = C_{db1} + C_{db2} + \frac{C_{gd2}}{2}. \quad (1)$$

The gate-to-drain capacitor in this equation is scaled by two since the gate-drain and gate-source capacitors of M_2 are connected in series as a result of the large resistor in series with the gate. C_g in Fig. 2 is the series combination of the gate-drain and gate-source capacitors of M_1 and given by $C_{gs1}/2$.

Assuming R_S is equal to R_L, we now can write the IL equation for the network as

$$IL = \frac{R_S}{\frac{R_S+R_{\rm on}}{2}} \frac{(1+sC_gR_{\rm on})}{(1+sC_TR_S)\left(1+s\frac{(C_T+2C_g)R_{\rm on}R_S}{2R_S+R_{\rm on}}\right)}. \quad (2)$$

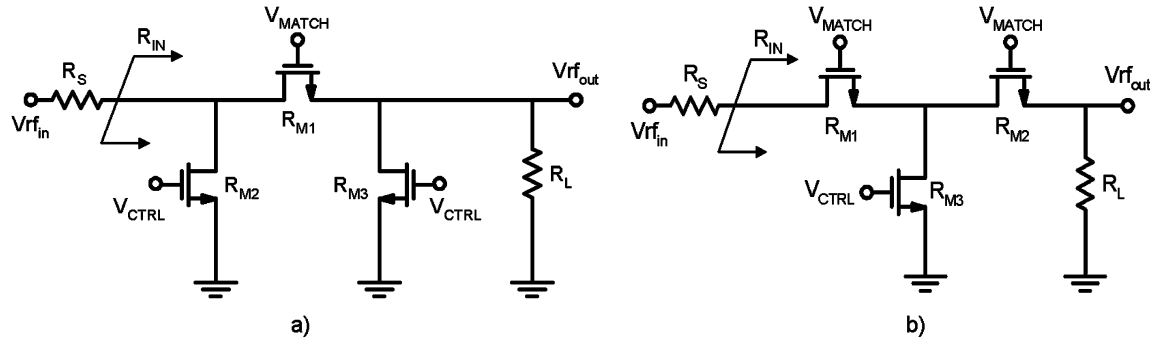

Fig. 1. Attenuator networks. (a) Π-Network. (b) T-Network.

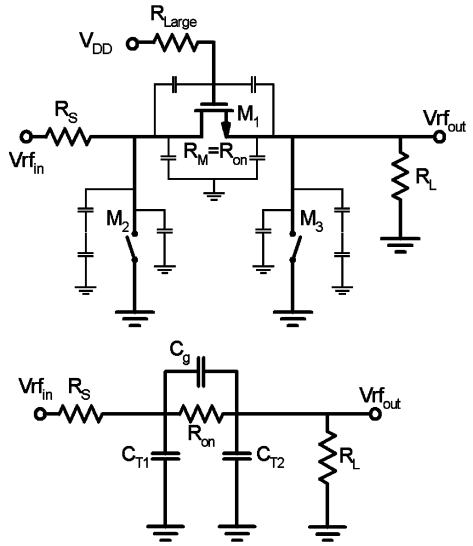

Fig. 2. Minimum insertion loss condition for a Π-Network and the equivalent circuit model.

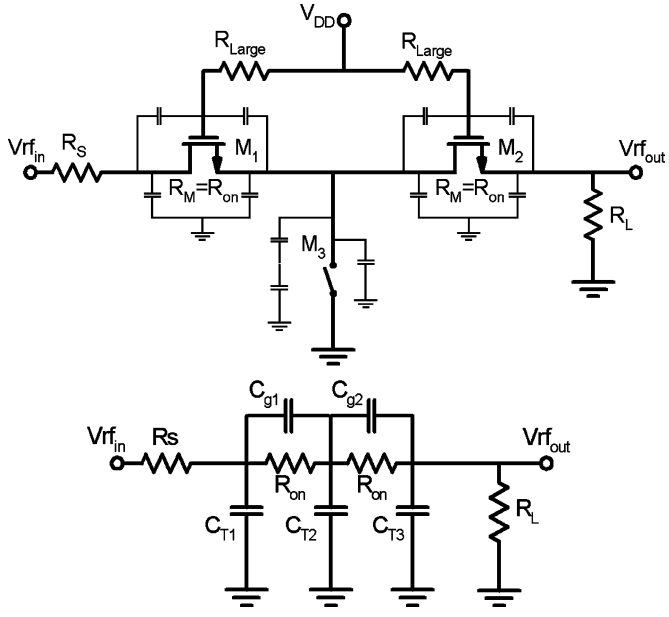

Fig. 3. Minimum insertion loss condition for a T-Network and the equivalent circuit model.

The first part of this equation gives the insertion loss of the network at low frequencies. $R_{\rm on}$ in (2) can be approximated by [2], [9]

$$R_{\rm on} = \frac{1+\theta(V_{GS}-V_t)}{\mu C_{\rm ox}\left(\frac{W}{L}\right)(V_{GS}-V_t-\eta V_{DS})} \tag{3}$$

where θ models the drain and source resistances, mobility degradation and other short channel effects. The exponential increase of the drain current with V_{GS} value in the subthreshold region is modeled by the parameter η.

In a fashion similar to the Π-Attenuator, the series devices of the T-Attenuator at the minimum gain setting are completely on and the shunt device is turned off. The loss in the attenuator is now dependent on the two series resistors, and the sizes of these resistors determine the amount of the loss. Fig. 3 shows the T-Attenuator in its minimum insertion loss setting. As mentioned previously for the Π-Attenuator, the capacitors in this figure denote the gate-oxide capacitors and the junction capacitors of the MOS devices. The lumped resistor-capacitor network equivalent of the schematic is also given in this figure.

We can conclude from the symmetry of the attenuator that C_{T1} is equal to C_{T3} and C_{g1} is equal to C_{g2}. These capacitors can be approximated as

$$C_T = C_{T1} = C_{T3} = C_{db1} \tag{4}$$

$$C_g = C_{g1} = C_{g2} = \frac{C_{gd1}}{2} = \frac{C_{gs2}}{2} \tag{5}$$

$$C_{T2} = C_{sb1} + C_{db2} + C_{db3} + \frac{C_{gd3}}{2}. \tag{6}$$

The transfer function for the circuit can be approximated for fairly small $R_{\rm on}$ at the minimum attenuation setting as

$$IL = \frac{R_S}{R_S+R_{\rm on}} \frac{1}{\left(1+s\left(C_T R_S + C_{T2}\frac{R_S+R_{\rm on}}{2}\right)\right)}. \tag{7}$$

The frequency independent term in (2) and (7) gives the IL for the attenuator at low frequencies. The dominant pole causes the IL to degrade at higher frequencies. The pole magnitude is set by the sum of all the parasitic capacitors from any node in the attenuator to ground, with the assumption that $R_{\rm on}$ is much smaller than R_S and R_L. Therefore, minimizing the total parasitic capacitors to ground in both of the attenuators will extend the bandwidth for the IL. Using large gate resistors serves this purpose as a result of isolating the gate capacitors of the series devices from input to output rather than being terminated

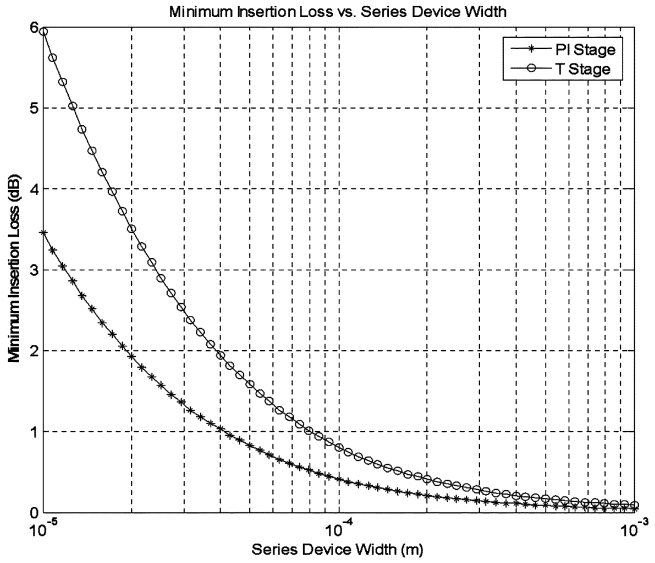

Fig. 4. IL versus series device width for the Π- and T-Attenuators at DC.

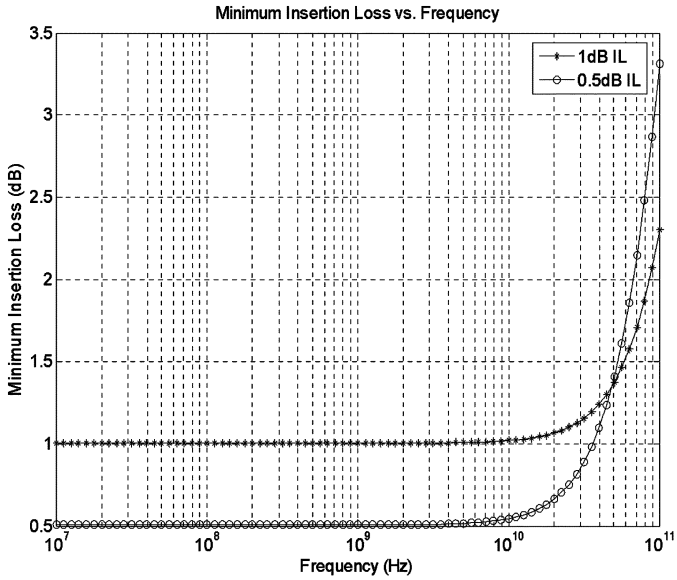

Fig. 5. IL versus frequency for the Π-Attenuator ($W_{\rm Series} = 40\ \mu$m, 80 μm).

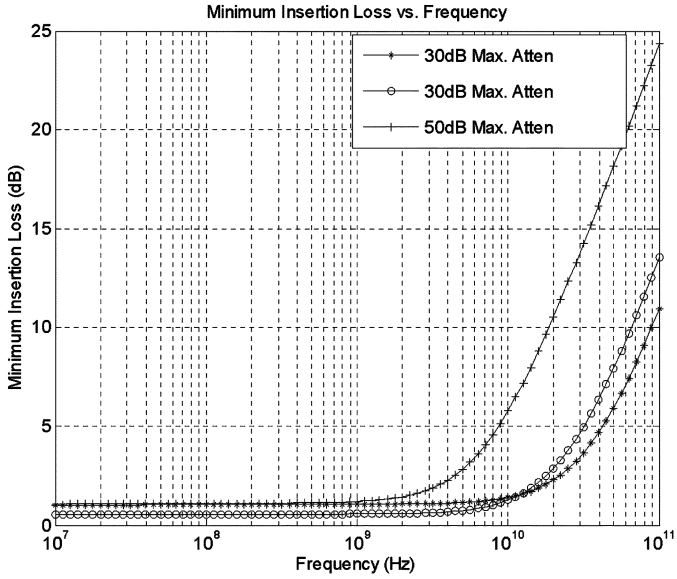

Fig. 6. IL versus frequency for the T-Attenuator ($W_{\rm Series} = 80\ \mu$m, 160 μm).

to ground. Furthermore, as explained previously, a tradeoff between the IL and the flatness of IL over frequency is apparent since increasing the device size to improve the IL introduces larger parasitic capacitors, which limit the bandwidth of the circuit.

T-type attenuators mainly achieve attenuation by shorting the middle node of the circuit in Fig. 3 to ground with the help of the MOS device M_3. Minimizing the on-resistance of this device increases the maximum achievable attenuation. Therefore, in this type of a network, the shunt device is usually made large. In addition, the series devices are chosen large to minimize the IL of the attenuator. Thus, the T-Attenuator has three large devices whose parasitic capacitors add up to give the dominant pole of the system. As a result, the total parasitic capacitance in this network is much larger than the Π-Network, resulting in a frequency response that is not as broad as in the latter. This is apparent in Figs. 5 and 6. Furthermore, as in the Π-Attenuator, for high impedance systems, finite shunt device off-resistance becomes comparable with the source resistance. This causes the series device resistance to increase and compensate for the reduced impedance for adequate matching, which increases the insertion loss for all frequencies.

Fig. 4 shows the simulated IL of the Π-Attenuator and T-Attenuator together as a function of the series device size. This graph verifies that for a given device size, the T-Network has larger loss and the IL improves with increasing device sizes. Figs. 5 and 6 show the simulated IL curve as a function of frequency for different low frequency IL and maximum attenuation settings. As shown by (2) and (7), the IL shows a single dominant pole roll off. In addition, improving the IL from 1 dB to 0.5 dB lowers the corner frequency of the attenuator. Similarly, increasing the shunt device size in the T-Network to improve maximum attenuation has a very large impact on the corner frequency due to increased parasitic capacitance in the circuit.

B. Maximum Attenuation

In the case of maximum attenuation, the series device in the Π-Attenuator completely shuts off, isolating the output from the input. At lower frequencies, almost complete isolation can be achieved from this topology. However, the leakage of the channel and additional parasitic resistances and inductances from the circuit ground to the common ground limit the isolation of the attenuator even at lower frequencies, since these create additional coupling paths from the input to the output. However, the isolation achieved from this kind of an attenuator with careful chip planning may be adequate for almost all applications owing to very high off-resistances of the MOS devices.

Fig. 7 gives the equivalent circuit for the Π-Attenuator for the maximum attenuation condition. The series device in this schematic is modeled by a resistance, $R_{\rm Series}$, and a capacitor, C_g, that form a feedthrough path from the input to the output.

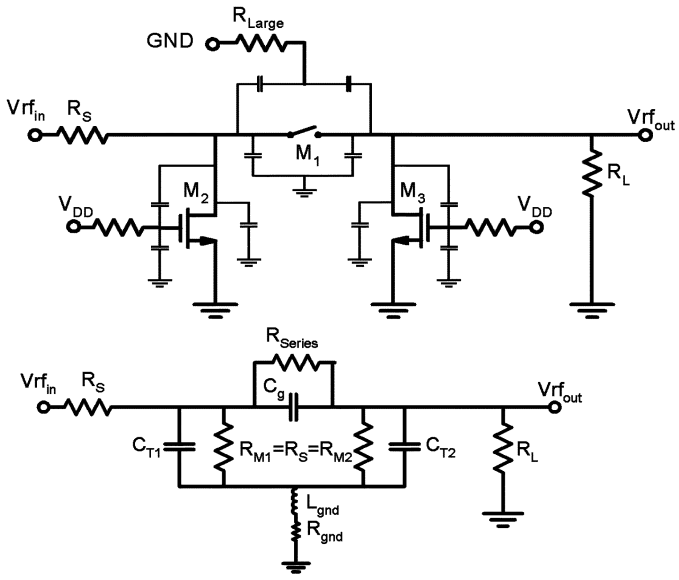

Fig. 7. Maximum attenuation condition for the Π-Network and the equivalent circuit model.

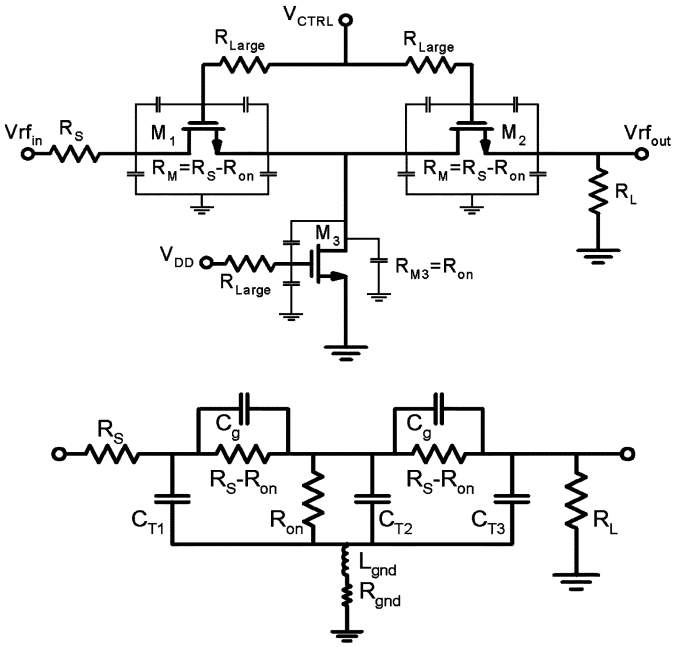

Fig. 8. Maximum attenuation condition for the T-Network and the equivalent circuit model.

It can be seen by inspection that if the resistance of the series device is infinite when it is off, this feedthrough capacitor gives a zero in the transfer function at DC. The shunt devices have channel resistances equal to R_S and R_L assuming perfect matching at DC and a large R_{Series}.

Capacitors in this network can be given as

$$C_T = C_{T1} = C_{T2} = C_{db1} + C_{db2} + \frac{C_{gd2}}{2} \tag{8}$$

$$C_g = \frac{C_{gd1}}{2}. \tag{9}$$

It is important to realize that values of these capacitors are dependent on the biasing of the transistor, therefore in each analysis they need to be handled carefully. In the off state, the device gate capacitor consists of the overlap capacitors, whereas in the on state, the capacitor is composed of the overlap and the gate oxide capacitors. Similarly the junction capacitors are functions of the transistor biasing.

We now can write the maximum attenuation achievable from $V\text{rf}_{\text{in}}$ as

$$\frac{1}{\text{Att}_{\text{MAX}}} = R_S \frac{Z_S(2Z_{\text{gnd}} + Z_S) + Z_{\text{Series}}Z_{\text{gnd}}}{(2Z_{\text{gnd}} + Z_S + R_S)(2Z_S R_S + Z_{\text{Series}}R_S + Z_{\text{Series}}Z_S)},$$

$$Z_S = \frac{R_S}{1 + sC_T R_S},$$

$$Z_{\text{Series}} = \frac{R_{\text{Series}}}{1 + sC_g R_{\text{Series}}},$$

$$Z_{\text{gnd}} = R_{\text{gnd}} + sL_{\text{gnd}}. \tag{10}$$

It can be shown from this equation that in the absence of any ground parasitics, the gain has a zero at $(-1/C_g R_{\text{Series}})$ and low frequency gain from the input of the attenuator is

$$\frac{1}{\text{Att}_{\text{MAX}}} = \frac{R_S(2R_{\text{gnd}} + R_S) + R_{\text{Series}}R_{\text{gnd}}}{2(R_S + R_{\text{Series}})(R_{\text{gnd}} + R_S)} \approx \frac{R_{\text{gnd}}}{2(R_{\text{gnd}} + R_S)}. \tag{11}$$

It is easy to show that the two poles in the transfer function are around $2/R_S C_T$ in the absence of ground parasitics. Given that the shunt devices (therefore C_T) are small, this pole magnitude is much higher than the useful frequency range of this network. Consequently, the maximum attenuation of the Π-Network becomes flat over a wide frequency range until the zero becomes effective at the frequency of $(-1/C_g R_{\text{Series}})$.

The T-Attenuator has slightly different performance from the Π-Attenuator for the maximum attenuation setting. When the isolation is maximum, the series devices have equivalent resistances close to R_S and R_L, and the shunt device is completely on with a very small channel resistance. The size of the shunt resistance determines the maximum attenuation value since smaller resistance corresponds to better grounding of the intermediate node.

Fig. 8 gives the equivalent circuit for the maximum attenuation setting of a T-Attenuator. The T-Attenuator in this condition is fairly wideband since the intermediate node has a very small resistance to ground and the capacitors connected to this node have very small time constants, therefore the transfer function has very high pole magnitudes. Parasitic capacitors at the input and output nodes consist only of the junction capacitors, thus the total parasitic capacitors at these nodes are relatively

small. Consequently, from a qualitative point of view, this network has a very wide frequency response in the maximum attenuation case. Capacitor values in this network are given in (4), (5) and (6). As mentioned previously, these capacitors are functions of the biasing of the transistors and therefore are different in value from the minimum attenuation case.

Assuming that $R_{\rm on}$ is much smaller than R_S, maximum attenuation for this network from $V{\rm rf}_{\rm in}$ can be approximated as

$$\frac{1}{\mathrm{Att}_{\mathrm{MAX}}} = \frac{Z_S^2(Z_{T2}+Z_{\rm gnd})}{R_S(Z_S+Z_{\rm Series})\,(2Z_{T2}+2Z_{\rm gnd}+Z_S+Z_{\rm Series})},$$
$$Z_S = \frac{R_S}{1+sC_TR_S},$$
$$Z_{T2} = \frac{R_{\rm on}}{1+sC_{T2}R_{\rm on}},$$
$$Z_{\rm Series} = \frac{R_S-R_{\rm on}}{1+sC_g(R_S-R_{\rm on})},$$
$$Z_{\rm gnd} = R_{\rm gnd}+sL_{\rm gnd}, \tag{12}$$

and the low-frequency gain of the network is given by

$$\frac{1}{\mathrm{Att}_{\mathrm{MAX}}} = \frac{R_S^2(R_{\rm on}+R_{\rm gnd})}{2R_S(2R_S-R_{\rm on})(2R_S+2R_{\rm gnd}+R_{\rm on})} \approx \frac{R_{\rm on}+R_{\rm gnd}}{2R_S}. \tag{13}$$

If we assume that the C_g and C_T values are close to each other and ground termination is ideal, (12) suggests that the gain of the system increases, or equivalently the attenuation drops with increasing frequency. However, it is important to realize that the pole and zero magnitudes for the attenuator are fairly large given that R_S is 50 Ω and C_T and C_g are small parasitic device capacitors. Therefore, the frequency response of the attenuator is flat in a very wide frequency range.

Fig. 9 gives the maximum attenuation of a Π-Network for two different IL values. Improving the IL by increasing the series device size increases the size of C_g in Fig. 7, therefore the maximum attenuation value at a given frequency degrades as a result. The flat parts of the curves are as a result of the nonzero off-resistance of the MOS device. Increasing the size of the device decreases this leakage resistance while increasing C_g. Consequently, the zero magnitude stays the same in the two curves. This figure also shows the effect of parasitic resistance and inductance in the ground path, namely at the source terminals of M_2 and M_3. The curves suggest that a parasitic resistance of 1 Ω limits the DC isolation by creating a path from input to the output, in the M_2–M_3 path. Isolation degrades 6 dB for each time this parasitic resistance doubles. Similarly, a parasitic inductance in the ground path causes limited isolation. It causes a low frequency pole which is a function of R_S and $R_{\rm Series}$ in the attenuation transfer function and maximum attenuation degrades 20 dB per decade as a result as shown in Fig. 9.

Fig. 10 gives the maximum attenuation as a function of frequency for the T-Attenuators. Five different plots are for three attenuators with different IL and maximum attenuation settings. The curves are flat over a very wide frequency range and eventually start rising as expected. Even for the case where the shunt

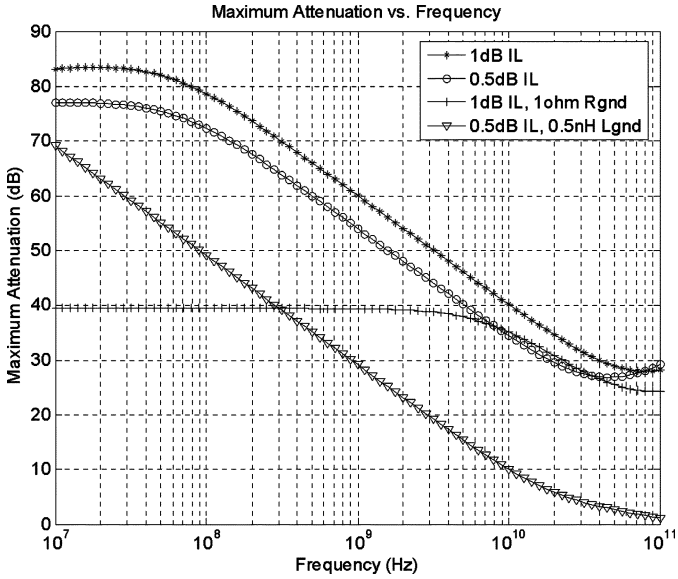

Fig. 9. Maximum attenuation versus frequency for the Π-Attenuator.

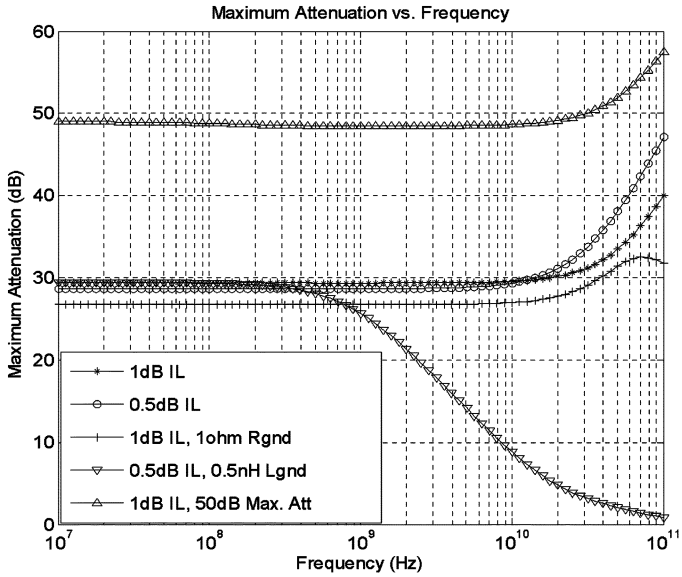

Fig. 10. Maximum attenuation versus frequency for the T-Attenuator.

device size is increased ten times to improve the maximum attenuation by 20 dB, the flatness of the curve persists because of the reasons given above. We can safely conclude from this graph that the maximum attenuation is flat in the useful frequency range. Effect of parasitic ground resistance and inductance is also shown on this plot. Parasitic resistance simply adds to the on-resistance of M_3, therefore limits the isolation for reasons given in this section. If the parasitic resistance is equal to M_3 on-resistance, this degradation becomes 6 dB. In the case of parasitic inductance, this inductance creates a pole approximately $R_{{\rm on},M3/2\pi L_p}$ in the attenuation transfer function.

It is apparent from Figs. 9 and 10 that maximum attenuation is vulnerable to any parasitic elements in the ground path. Therefore, careful layout planning is particularly important in these systems and multiple stages should always be considered for adequate isolation.

C. Impedance Matching

In this section, we limit our analysis to variations from ideal matching due to high frequency effects. For this purpose, we make the assumption that at low frequencies, best possible matching is achieved between the source impedance and the input impedance of the attenuator and similarly between the load impedance and the output impedance of the attenuator. For instance, at the lowest attenuation setting of the Π-Attenuator, best possible matching is in fact not perfect since the source impedance matches to the sum of on-resistance of the series device and the load resistance. Therefore, perfect matching cannot be achieved and we will refer to "best possible matching."

Given that the block we are dealing with is a wideband system, the match at low frequencies is resistive. As we move to higher frequencies, the parasitic capacitors of the devices start degrading the matching of the system. Since the operating point of each device in the attenuator depends highly on the attenuation amount, it is necessary to find a worst-case scenario. This worst case can be identified as the minimum attenuation setting for both attenuator types since it can easily be seen that when the on-resistance $R_{\rm on}$ of the series device approaches zero, the input, output and any internal nodes are shorted to each other. The total parasitic capacitors at these nodes are summed up and form a single dominant pole. Therefore, in this operating condition, the dominant pole magnitude for the S11 response of the attenuators becomes the smallest, limiting the frequency response of the system.

In light of this conclusion, we now can estimate the input impedance of the Π-Network given in Fig. 2 using (A1) and assuming a small $R_{\rm on}$ as

$$Z_{\rm in\Pi} \approx \frac{R_L + R_{\rm on}}{1 + s2C_T R_L}. \tag{14}$$

C_T in this equation is given in (1). It is clear from (14) that, to the first order, the dominant pole magnitude for the input impedance of the network scales with the total parasitic capacitors in the network that are terminated at the ground. Therefore, minimizing the capacitors to ground broadens the frequency response of the system, as in the minimum IL case. This is partly achieved by shunting gate capacitors of the series devices to the output using $R_{\rm Large}$.

Similarly, the input impedance of the T-Network for worst-case matching in Fig. 3 can be estimated using (A2) and assuming a small $R_{\rm on}$ as

$$Z_{\rm in} = \frac{R_L + 2R_{\rm on}}{1 + s(2C_T + C_{T2})R_L}. \tag{15}$$

This equation verifies that the network has a single dominant pole that is a function of all the parasitic capacitors in the system that are terminated at ground in a manner similar to the Π-Attenuator case. Equation (15) is an approximate result and is valid in the useful frequency range of the attenuator. We define this useful frequency range as S11 equal to or better than $-10\,\rm dB$, which is a commonly accepted limit for a reasonable matching to the desired impedance.

Fig. 11 shows the simulated low frequency S11 response of the T and Π-Attenuators as a function of the series device width. The trend of the plot is mainly due to the fact that increasing the device size decreases the channel resistance of the device that is in between the source and load impedances. The curve for the T-Attenuator is shifted up since there are two series resistors in this network. By way of making the series resistor smaller, the source matches to the load better, improving the matching of the system. However, increasing the device sizes in return degrades the frequency response of the S11 parameter as shown in Figs. 12 and 13.

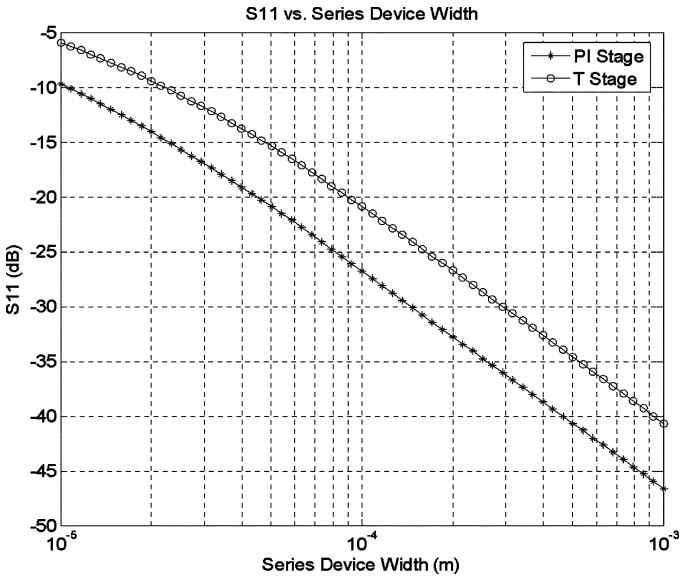

Fig. 11. S11 versus series device width for the T and Π-Networks at minimum attenuation at DC.

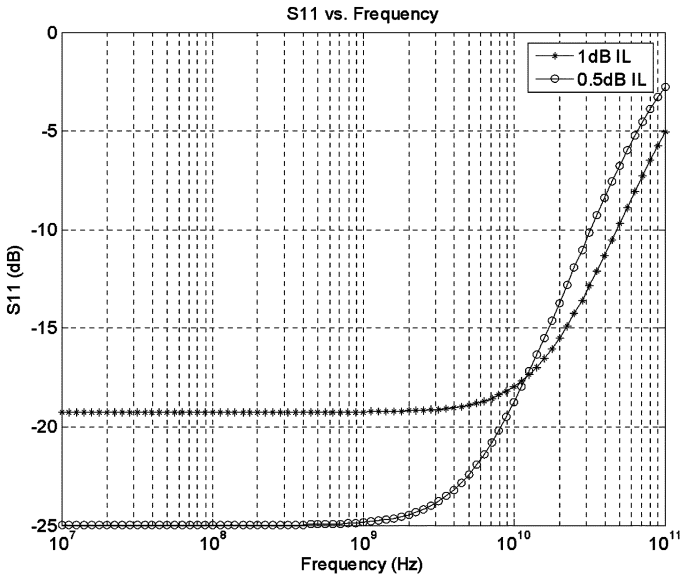

Fig. 12. S11 versus frequency for the Π-Network in the minimum attenuation mode.

Fig. 12 shows that although increasing the series device size to improve the IL of the attenuator improves the low frequency S11 response, the pole of the input impedance given by (14) moves to a smaller magnitude. As a result, the frequency corner of the Π-Attenuator degrades as shown in this figure. Similarly, Fig. 13 shows the S11 response of the T-Network as a function of frequency. It is also evident from this plot that as the device

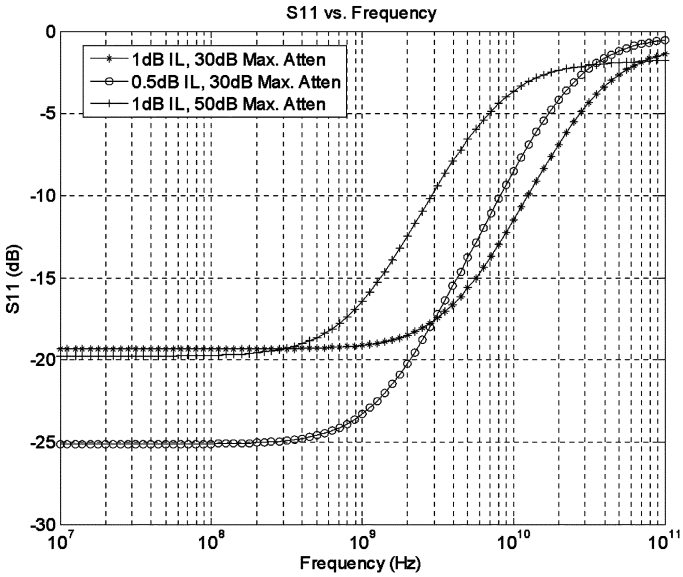

Fig. 13. S11 versus frequency for the T-Network in the minimum attenuation mode.

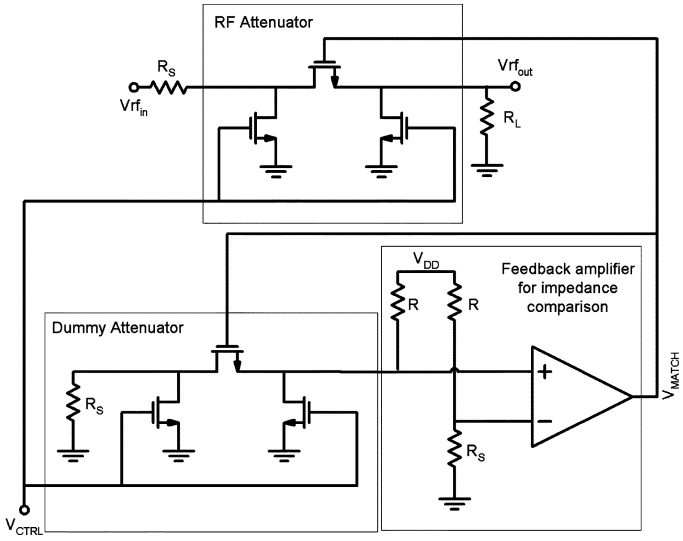

Fig. 14. Circuit schematic of the impedance matching feedback network.

sizes increase in the network, the corner frequency for adequate matching degrades. Improving the maximum attenuation by 20 dB via increasing the shunt device size ten times reduces the frequency corner dramatically as shown in the graph.

D. Impedance Matching Feedback Loop

In order to match to the desired impedance at the input and output ports of the attenuator as the gain of the system varies, a feedback system needs to be incorporated in the design. The feedback senses any variation from the ideal matching condition and forces the system to compensate for the changes. The shunt devices in the attenuator types we analyzed are typically used to compensate for the change in the series device as the signal is attenuated. Therefore, while an external control voltage controls the series device channel resistance, a feedback control voltage controls the channel resistance of the shunt devices.

In order not to disturb the operation of the RF attenuator with the impedance matching network, a dummy replica attenuator is used to sense and correct the impedance via the generation of a feedback voltage. The control voltage along with the feedback voltage then can be applied to the RF attenuator to match while attenuating.

Fig. 14 gives the circuit diagram of a RF attenuator with the feedback control loop used for matching to the source and load impedances [6]–[8]. The resistors R and R_S form a voltage division branch from $V_{\rm DD}$ to ground resulting in a DC voltage at the negative operational amplifier (opamp) input. This voltage is compared to the voltage at the positive input, which is generated by the voltage division of the resistor R and the equivalent DC resistance of the replica attenuator. R_S resistors in the feedback loop are on-chip components with values equal to the input source resistance. Deviation in the values of these resistors as a result of process drift degrades the impedance matching of the RF attenuator. However, S11 is still better than -10 dB even with 50% drift in these resistor values. The feedback amplifier compares the voltages between its two inputs and the error signal across the two inputs of the amplifier generates the feedback voltage identified as $V_{\rm MATCH}$. This feedback voltage is then applied back to the attenuator in order for the feedback to minimize the error signal. Consequently, as varying $V_{\rm CTRL}$ changes the attenuation of the network, the feedback network adjusts the value of $V_{\rm MATCH}$ to keep the low frequency input and output impedances of the attenuator block constant and equal to R_S value. The same control voltages are applied to the RF attenuator to get the same attenuation and matching characteristics.

Applying the control voltage to the shunt device as opposed to the series device has its advantages. First, at the minimum attenuation setting, the shunt device is driven at the gate with 0 V as opposed to the feedback voltage, which settles down to a nonzero voltage. This limits the additional loss due to the shunt devices. Additionally, when the control voltage is less than the threshold voltages of the shunt devices, these devices operate in the subthreshold region where their characteristics are exponential. Therefore, the attenuator responds in a linear-in-dB fashion to the control voltage at low attenuation settings, meaning the attenuation in dB increases linearly with the control voltage, which is highly desirable for attenuators. This is shown in detail below.

Linear-in-dB attenuation curve is generally much desired in communication systems. The slope of the attenuation curve usually determines the resolution that can be achieved in the gain control and if this slope is very high in some regions and very low in others, it becomes troublesome to estimate the level of gain control with the control voltage. Especially in high slope regions, small variations in the control voltage result in large variations in the gain of the system. Overall, a gain curve with very large and slow regions requires very high dynamic range in the gain control loop, which is not desirable. Once a relatively linear-in-dB gain control curve is achieved by design, the gain control loop can easily be calibrated to compensate for variations in the slope.

In order to find the attenuation equation as a function of the control voltage for the Π-Network given in Fig. 1(a), we can

start by writing the low-frequency equivalent input impedance of the system. In calculating the input impedance, we will start out assuming R_{M2} is equal to R_{M3} and R_L is equal to R_S. Then, using (A4)–(A6), the attenuation equation can be written as

$$\frac{1}{\text{Att}} = \frac{R_{M2} - R_S}{R_{M2} + R_S} \tag{16}$$

where R_{M2} is given by (17), which gives the derivative of the drain current as a function of the drain-source voltage [2]

$$R_{M2} = \frac{\partial I_D}{\partial V_{DS}} = \frac{\partial}{\partial V_{DS}} \left(K \left(\frac{X_1^2 - X_2^2}{1 + \theta X_1} \right) \right) \tag{17}$$

$$K = \mu C_{\text{ox}} \frac{W}{2\eta L} \tag{18}$$

$$X_1 = 2\eta\phi_t \ln(1 + e^{(V_{GS} - V_T)/(2\eta\phi_t)}) \tag{19}$$

$$X_2 = 2\eta\phi_t \ln(1 + e^{(V_{GS} - V_T - \eta V_{DS})/(2\eta\phi_t)}). \tag{20}$$

The control voltage is applied to the gate of the shunt transistors and the V_{GS} value in (19) and (20) is equal to V_{CTRL}, assuming the bias voltages at the input and output are set to 0 V. The device equation used in (17) is explained in detail in [2]. Logarithm of inverse of (16) gives the attenuation in dB scale. We can easily find the criteria for linear-in-dB gain control for the attenuator simply by taking the derivative of dB scale attenuation equation. It can be shown that such a condition holds true when $\left(\partial R_{M2}/\partial V_{\text{CTRL}}/R_{M2}^2 - R_S^2\right)$ is constant for all V_{CTRL} values.

Fig. 15 gives the simulated attenuation of the Π-Network as a function of the control voltage. As mentioned previously, linear-in-dB attenuation is desirable in gain control blocks. Fig. 15 shows a linear response to the control voltage in the first 25–30 dB attenuation range. In the first parts of the attenuation curve, the shunt device is in weak and moderate inversion displaying the exponential characteristics and the series device is in strong inversion, resulting in a linear gain control curve. In the latter parts of the attenuation curve, the shunt device becomes linear and the series device is exponential resulting in an increased gain change with control voltage.

Fig. 15 omits any frequency and parasitic resistance effects in the attenuation curve. First, the feedforward capacitance due to the series device in the Π-Attenuator limits the maximum attenuation at higher frequencies, limiting the tail of the curve in Fig. 15 at higher frequencies. This is desirable in most cases since the nonlinear part of the curve is shifted up resulting in a more linear overall curve.

Second, on-chip parasitic resistors limit the attenuation curve at higher attenuation settings. The most dominant of these resistors is the one from the attenuator ground to absolute ground. If the attenuator is not well grounded, this creates an additional feedthrough path from the input to output via the shunt devices. These effects also shift the curve in Fig. 15 up at the higher attenuation region. Consequently, when frequency and on-chip parasitic effects take effect, the attenuation curve becomes more linear as shown in measured attenuator data in Section III.

In order to find the attenuation curve for the T-Attenuator we can do a similar analysis as was done for the Π-Attenuator. Fig. 1(b) shows the T-Network with the bias voltages applied to the gates of the devices. In a manner similar to the Π-Attenuator case, the control voltage is applied to the shunt device and the feedback voltage controls the series devices.

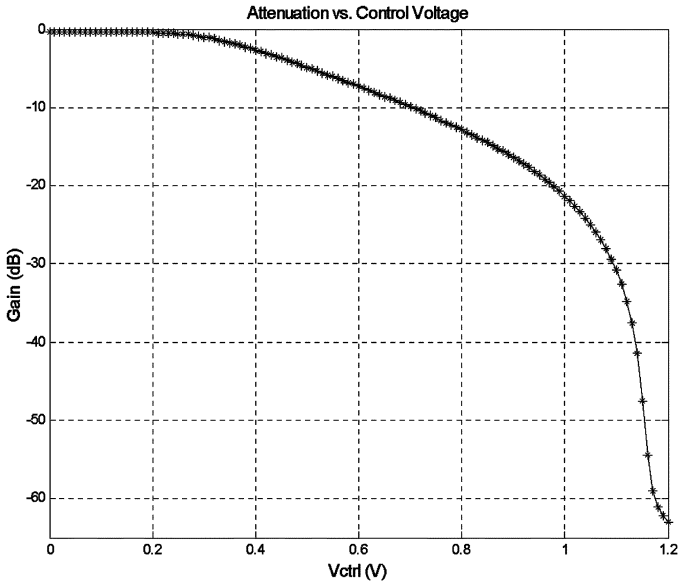

Fig. 15. Attenuation versus control voltage for a Π-Attenuator.

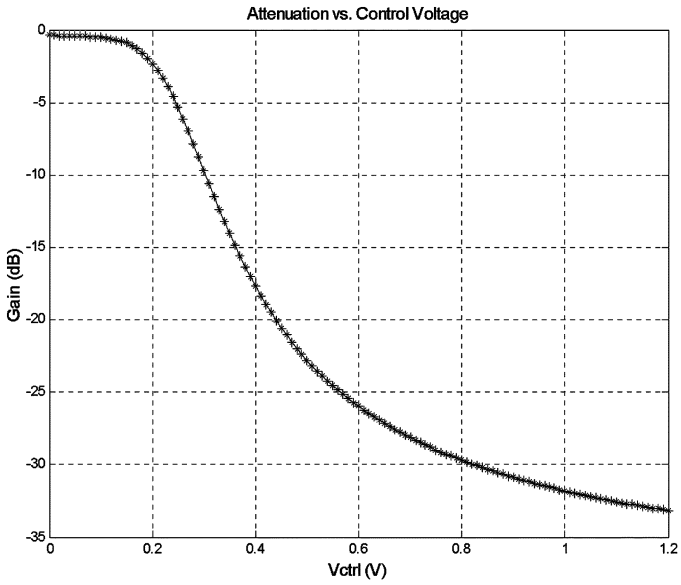

Fig. 16. Attenuation versus control voltage for a T-Attenuator.

With the same assumptions as in the previous section and using (A7)–(A9), we can write the attenuation equation for a T-Network as

$$\frac{1}{\text{Att}} = \frac{R_{M3}}{R_S + \sqrt{R_{M3}^2 + R_S^2}} \tag{21}$$

where R_{M3} is given as similar to (17).

Fig. 16 shows the simulated attenuation curve as a function of the control voltage. The curve is linear in the first part because of the reasons given for the Π-Attenuator. Namely, the shunt device in its exponential region gives a linear-in-dB response in the first 20 dB of attenuation. In the second part of the curve, unlike the Π-Attenuator, the gain changes slower with the

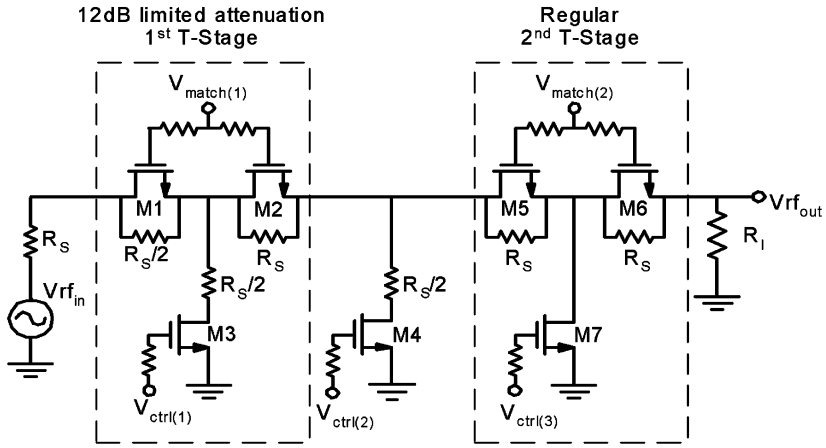

Fig. 17. Two-stage cascaded T-Attenuator circuitry with limited attenuation first stage and regular second stage.

control voltage. This is mainly due to the fact that attenuation is achieved by the change in the shunt device resistance, and in the latter parts of the curve in Fig. 16 the shunt device operates in strong inversion region, slowing the rate of change of the attenuation curve with the control voltage.

III. Attenuator Design Example

A. Design Methodology

The analysis of the attenuators in the previous section showed that with the advancements in CMOS technology, it is possible to design attenuators with multi-gigahertz frequency corners. It has also been shown in the literature that Π-Attenuators with good IL and isolation can even be designed to work as high as 10 GHz with the technology used in this paper [3]. In the rest of this publication, we will focus our attention to trying to trade off available bandwidth with another equally important design parameter in attenuators, linearity.

It has been shown in [2] that T-Networks in general are more linear than the Π-Networks, especially at higher attenuation settings. It has also been proved in the same work that forcing the series devices in a T-Network to turn off at higher attenuation settings improves the linearity of the network further, since these devices no longer generate distortion. The attenuator presented here makes use of this fact along with other design techniques to trade off bandwidth with linearity.

Fig. 17 shows the generalized circuit diagram of the proposed attenuator design. The design consists of two T-stages cascaded and utilizes an asymmetric approach rather than the traditional symmetric approach to attenuator design. In the case of minimum attenuation, the series devices are on and the shunt devices turn off. Consequently, the input and the output low frequency impedances are given by

$$Z_{\rm IN} \approx Z_{\rm OUT} \approx R_S + 4R_{\rm ON} \tag{22}$$

if we assume that $R_{\rm ON}$ is much smaller than R_S, and R_l is equal to R_S, thereby giving adequate matching to the source and load.

When the attenuator is in the maximum isolation setting, the series devices turn off, and the input and output impedances can be given as (23) and (24), respectively, therefore good matching

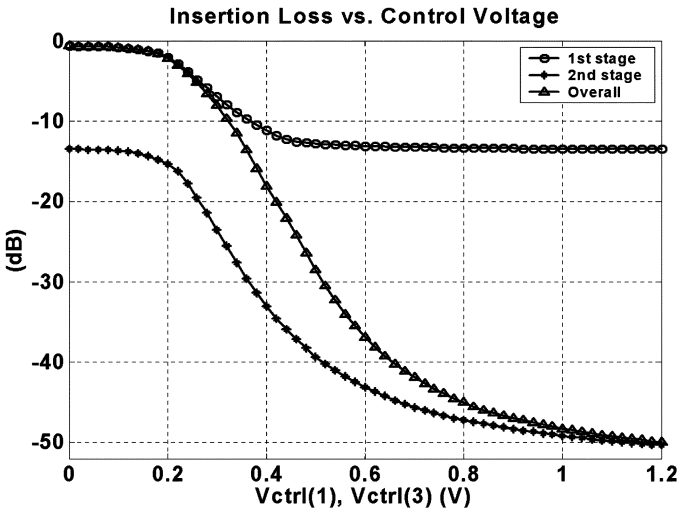

Fig. 18. Simulated attenuation versus control voltage for the two stages of the attenuator.

is achieved since M3 and M7 are large devices and have small on-resistances.

$$Z_{\rm IN} \approx \frac{R_S}{2} + \frac{R_S}{2} + R_{M3} \tag{23}$$

$$Z_{\rm OUT} \approx R_S + R_{M7}. \tag{24}$$

The use of shunt resistors across the series devices forces these devices to turn off at the maximum attenuation setting for good matching at the input and output ports. As mentioned above, since the series devices are off, they do not contribute any distortion when the attenuator moves closer to maximum attenuation. Furthermore, at maximum attenuation, the shunt devices are highly linear since their channel is strongly inverted and very small signal swing is present across their terminals due to their small on-resistance [2]. Overall, at high attenuation settings, the attenuator is highly linear. This is desirable for most applications since high attenuation corresponds to large incident power to the receiver.

Although the use of shunt resistors improves the linearity when close to the maximum attenuation, this improvement was shown to be limited to the last 5–10 dB attenuation range of attenuators that have isolation in excess of 30 dB [2]. It is very

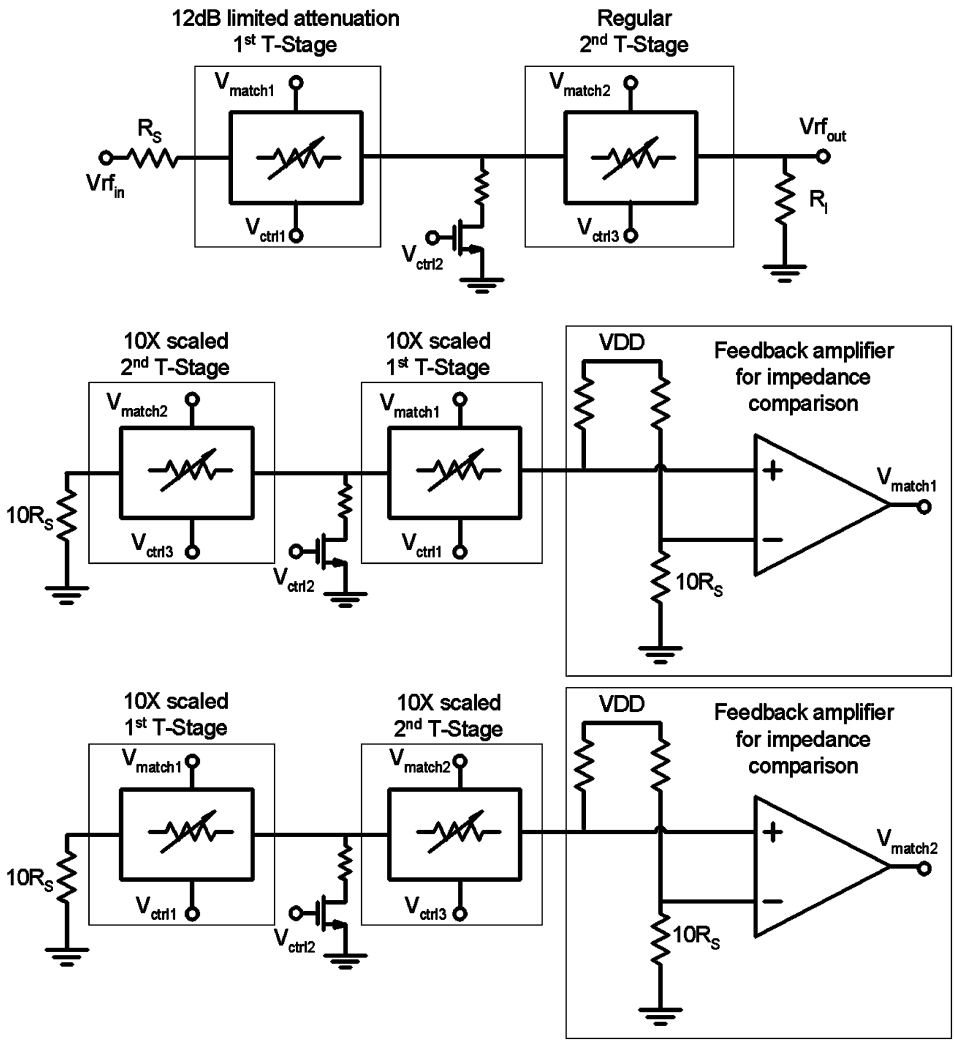

Fig. 19. Overall attenuator block diagram with RF attenuator and 10X scaled replica attenuators in impedance matching FB loops for the input and output ports.

desirable for such gain control blocks to improve their linearity in the first 5–10 dB attenuation range and stay highly linear in the rest of the gain range.

In order to achieve this desired response, the two stages in Fig. 17 attenuate the signal consecutively rather than concurrently. Initially the first stage starts attenuating, and the second stage is in its minimum attenuation mode. In this mode, the second stage is highly linear since the series devices are strongly inverted and the shunt devices are off. Once the first stage reaches its maximum attenuation, it is highly linear for the reasons discussed above and the second stage starts attenuating.

Maximum attenuation of the first stage in Fig. 17 is limited to around 12 dB. This is achieved by inserting two resistors of values $R_S/2$ in shunt with M1 and in series with M3. Fig. 18 shows the attenuation curve of the first and second stages with respect to $V_{\mathrm{ctrl}(1)}$ and $V_{\mathrm{ctrl}(3)}$, respectively. In this figure, second stage attenuation curve is drawn assuming the first stage is at maximum setting. The attenuation of the first stage reaches its maximum value of 12 dB when V_{ctrl1} reaches around 0.5 V. The second stage starts attenuating for $V_{\mathrm{ctrl}(3)}$ values of around 0.2 V. In the final design, around 100 mV and 200 mV were subtracted from $V_{\mathrm{ctrl}(1)}$, respectively, to generate $V_{\mathrm{ctrl}(2)}$ and $V_{\mathrm{ctrl}(3)}$. Shift voltage values were generated on-chip and simple opamp subtractors were used to generate $V_{\mathrm{ctrl}(2)}$ and $V_{\mathrm{ctrl}(3)}$. An attenuation curve dependent on a single control voltage was achieved as a result. The overall attenuation curve with respect to a single external control voltage, $V_{\mathrm{ctrl}(1)}$, is also shown in Fig. 18. Furthermore, the attenuation curve is monotonous and mostly independent of kinks in the presence of variation of shift voltage amplitudes due to process corners.

It can be shown that the overall linearity of two cascaded stages is approximately [12]

$$\frac{1}{\mathrm{IIP}_3^2} \propto \frac{1}{\mathrm{IIP}_{3,1}^2} + \frac{\mathrm{Att}^2}{\mathrm{IIP}_{3,2}^2}. \tag{25}$$

This equation suggests that the effective linearity of the second stage scales inversely with the attenuation (Att) of the first stage. Since the signal is attenuated by 12 dB before it reaches the second stage, the linearity of the second stage is improved by 12 dB. As a result, the linearity of the proposed attenuator design improves within the first 10–12 dB of attenuation.

Use of resistors to limit the attenuation range of the first stage degrades the frequency response of the attenuator, since the same attenuation can be achieved using a much smaller shunt

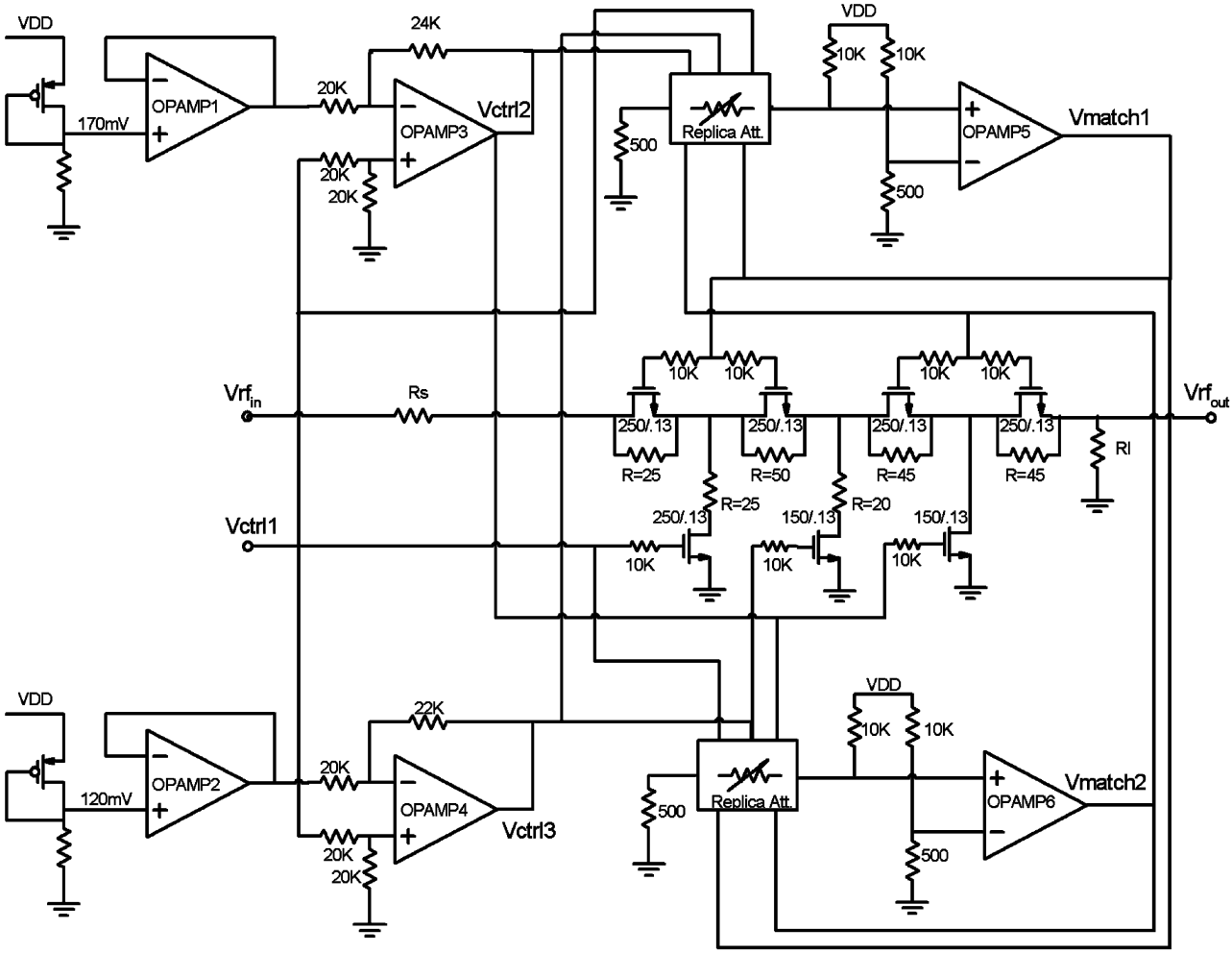

Fig. 20. Overall attenuator circuitry with control voltage generation.

device that has an on-resistance of $R_S/2$. Larger device sizes result in smaller on-resistance for the devices and using them along with the resistors as given in the design guarantees low signal voltage or current swing across the devices when the attenuator is in maximum attenuation setting. However, this in return causes larger parasitic capacitors in the circuit, which limits the frequency response. Furthermore, using T-Networks instead of the broader Π-Networks results in further degradation in frequency response. Consequently, the design presented in this section trades off bandwidth for linearity.

Fig. 19 gives the block diagram of the attenuator. The two feedback loops control the impedance of the input and output separately using replica attenuators and use $V_{\mathrm{match}(1),(2)}$ to match to R_S and R_L. Control voltages are applied to the shunt devices to obtain a linear-in-dB attenuation control as explained previously. The replica attenuator equivalent resistances were scaled up by 10X to reduce the die area (smaller devices) and power dissipation in the comparison branches. The DC bias voltage at the input and output of the RF attenuator was set to ground to maximize the overdrive (V_{GS}) values for the devices and hence minimize the IL. The comparison node voltages at the opamp input were set to around 60 mV by choosing the resistors in the comparison branches to be 10 kΩ and 500 Ω (10X scaled). This in return minimizes the resistance offset between the RF and replica attenuators due to DC differences at the drains and sources. Comparison amplifiers were designed to minimize input offset (using circuit and layout techniques such as large device sizes and cross-quad and interleaved layout) in order to reduce impedance matching error as a result of the low 60 mV comparison voltage.

Fig. 20 shows the final attenuator design schematic. Opamps 1 and 2 are used to buffer the shift voltages whereas 3 and 4 generate control voltages, $V_{\mathrm{ctrl}(2)}$ and $V_{\mathrm{ctrl}(3)}$. The design incorporates two interconnected feedback loops and local feedback loops in the control voltage generation circuitry. Each feedback loop was compensated to prevent any stability problems. Stability was verified extensively via simulations over all process and temperature corners. Simulated settling time was less than 1 μs from minimum-to-maximum attenuation and vice versa.

Other design parameters include noise performance and PSRR. Simulations showed that the noise figure (NF) of the attenuator is equal to the IL at the minimum attenuation mode and increases by 1 dB per dB of attenuation thereafter. Power supply rejection from V_{DD} is generally excellent since the signal path does not have a direct connection to the power supply. Only path from the power supply is through the control voltages, and these have the large gate resistors in front of them which block any leakage of power supply noise from the gate of the devices to the drain or the source. However, the design is susceptible to any ground noise coupling. Simulations

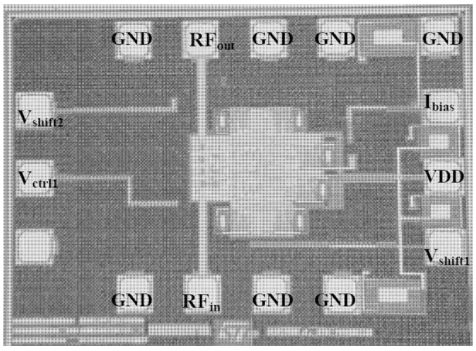

Fig. 21. Chip photograph. ($I_{\rm bias}$, $V_{\rm shift1}$ and $V_{\rm shift2}$ are generated on chip).

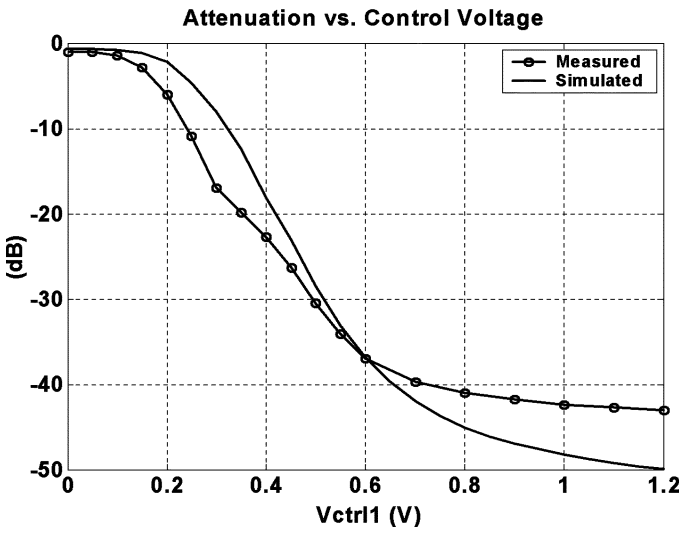

Fig. 22. Measured and simulated attenuation curves versus control voltage $V_{\rm ctrl1}$ for $f_{\rm signal} = 100$ MHz.

show very little rejection for the ground noise. To overcome this problem, very careful layout design and good termination of local ground to common ground is required. Also, with a differential approach, all supply noise can be rejected with good matching between differential components.

B. Experimental Results

The attenuator has been fabricated in a commercially available 0.13 μm digital CMOS technology. The chip measures 700×1000 μm^2 with all the bias generation integrated on chip. Measurements were made with cascade probes, a HP8719C Network Analyzer, a HP8563E Spectrum Analyzer and HP function generators. Fig. 21 shows the attenuator chip photograph.

Fig. 22 shows the attenuation curve with the control voltage when the input is at 100 MHz. Measured attenuation curves were quite independent of frequency, except for their higher insertion loss at higher frequencies. The attenuation curve is mostly linear-in-dB especially in the first 40 dB of attenuation. The slight kink in the measurement results is thought to be due to the poor choice of shift voltages and the variations in the process from typical corner.

Fig. 23 gives the minimum IL and maximum attenuation with frequency. The IL degrades from 0.9 dB to less than

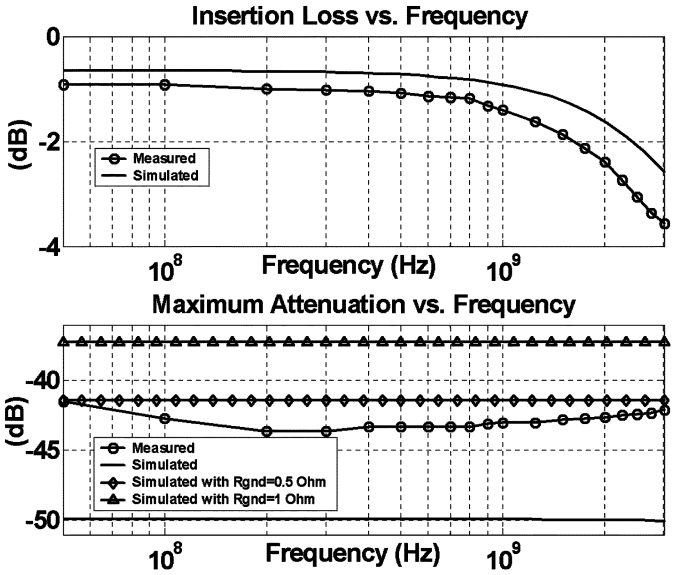

Fig. 23. Measured and simulated insertion loss and maximum attenuation versus frequency.

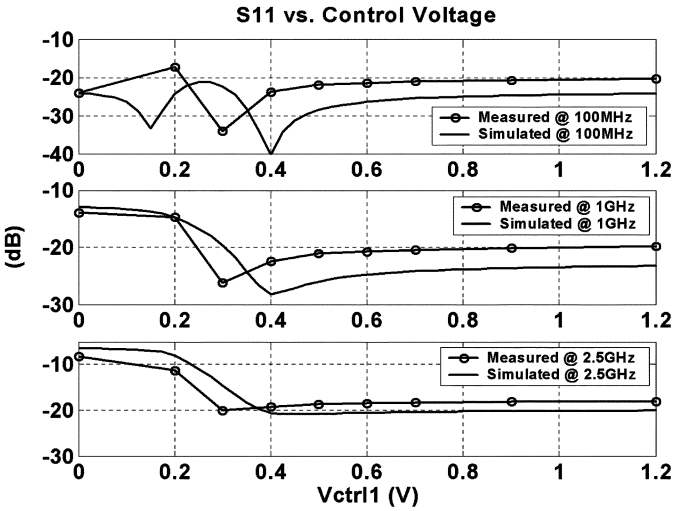

Fig. 24. Measured and simulated S11 parameter versus control voltage $V_{\rm ctrl}$ at 100 MHz, 1 GHz and 2.5 GHz.

3.5 dB from DC to 2.5 GHz. IL flatness is 1 dB in the frequency band of DC-1.5 GHz. The discrepancy from the simulated IL is most likely due to on-chip parasitics and modeling errors. The measured maximum attenuation is around 42 dB and flat with frequency as expected for T-configurations. The three simulated curves were generated with different parasitic interconnect resistor values from the attenuator ground to the actual chip ground. With 0 Ω parasitic interconnect resistor the designed maximum attenuation is around 50 dB. When the interconnect resistor is set to 0.5 Ω, simulated maximum attenuation drops down to 42 dB and similarly it drops down to 36 dB for an interconnect resistor of 1 Ω. To minimize the interconnect resistors, attenuator ground connections were laid out by stacking up available metal layers. Process variations and coupling to the output from substrate due to nonzero substrate resistance cause additional deviation from the simulated values.

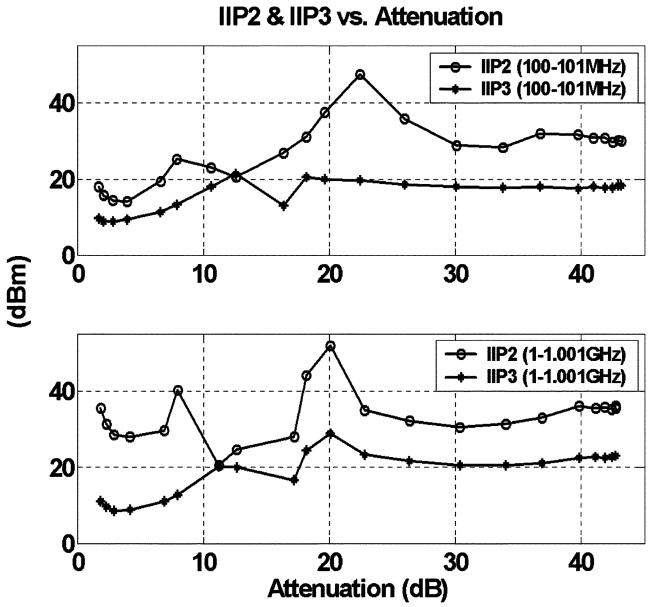

Fig. 25. Measured IIP2 and IIP3 results for two tones at 100–101 MHz and 1–1.001 GHz with 8 dBm and −3 dBm input power at lower and higher attenuation settings respectively for each tone.

Fig. 24 is a plot of S11 response of the attenuator at different attenuation settings and different frequencies. Worst case S11 is at minimum attenuation setting as explained in the previous section. Worst case S11 is −8.2 dB at 2.5 GHz for the minimum IL setting. S22 was measured to be as good as or better than S11 across all corners.

Fig. 25 gives the distortion performance of the attenuator in terms of IIP_2 and IIP_3 for two tones at 100 MHz-101 MHz and 1 GHz-1.001 GHz for the two graphs respectively. The input power to the attenuator was around −8 dBm for the lower attenuation settings and −3 dBm for the higher attenuation settings. The intermodulation distortion generation follows a similar trend for both the low and high frequency ranges, except that the linearity of the attenuator is slightly improved at higher frequencies. This is mainly due to the more effective gate bootstrapping at higher frequencies via the parasitic gate capacitors and the 10 kΩ resistors at the gates of the devices. It has been shown in the literature that modulating the gate of a triode-device with the average of the drain and source signal amplitudes help linearize the device [5]. It is verified with simulations that the two tone separation does not cause any variation in distortion products as long as these tones or the resulting products are within the bandwidth of the attenuator.

Fig. 25 shows that the linearity of the attenuator starts degrading as the first stage starts attenuating. This is mainly caused by turning on the shunt device, which starts generating distortion and decreasing the gate overdrive voltage of the series devices, which make them more nonlinear. However, as the gate overdrive voltage of the shunt device increases, its linearity improves. Moreover, decreasing the gate voltages of the series devices increase their channel resistance further, which cause the shunt fixed resistors to dominate and limit the distortion generation in those devices. As a result, the linearity improves again as the attenuation of the first stage increases to its maximum value. This process repeats itself for the attenuation range of the second stage, causing the second dip in the linearity curves. However, the linearity degradation is limited for the second stage because of the reasons given above in the circuit description part. As a result, improvement in distortion performance is observed at the higher attenuation settings. The distortion performance of existing attenuators shows IIP_2 and IIP_3 values of less than 10 dBm [3], [4]. With the present approach, the attenuator linearity is improved at higher attenuation settings allowing increased power handling. The 1 dB compression point of the attenuator was measured to be +2.5 dBm, which is the limit that the attenuator can handle.

The total power dissipation for the attenuator was 1.9 mW drawn from a 1.2 V power supply. Table I gives a summary of the performance spec for the attenuator.

APPENDIX

The input impedance of the Π-Network given in Fig. 2 is given in (A1) at the bottom of the page.

The input impedance of the T-Network given in Fig. 3 is given in (A2) at the bottom of the page, where Z_1 is given by

$$Z_1 = \frac{R_L(1+sC_gR_{\mathrm{on}}) + R_{\mathrm{on}}(1+sC_TR_L)}{(1+sC_gR_{\mathrm{on}})(1+sC_TR_L)}. \tag{A3}$$

The input resistance of the Π-Network can be given as

$$R_{\mathrm{IN}} = \frac{R_{M2}(R_{M2}R_S + R_{M1}R_S + R_{M1}R_{M2})}{R_S^2 + 2R_{M2}R_S + R_{M1}R_S + R_{M1}R_{M2}} = R_S. \tag{A4}$$

For an ideal match at the input, we can set R_{IN} given in (A4) equal to R_S. Solving this equation, R_{M1} can be written as a function of R_S and R_{M2} as

$$R_{M1} = \frac{2R_{M2}R_S^2}{R_{M2}^2 - R_S^2}. \tag{A5}$$

$$Z_{\mathrm{in}\Pi} = \frac{R_L(1+sC_gR_{\mathrm{on}}) + R_{\mathrm{on}}(1+sC_TR_L)}{(1+sC_gR_{\mathrm{on}})(1+sC_TR_L) + sC_TR_L(1+sC_gR_{\mathrm{on}}) + sC_TR_{\mathrm{on}}(1+sC_TR_L)}. \tag{A1}$$

$$Z_{\mathrm{in}T} = \frac{Z_1(1+sC_gR_{\mathrm{on}}) + R_{\mathrm{on}}(1+sC_{T2}Z_1)}{(1+sC_gR_{\mathrm{on}})(1+sC_{T2}Z_1) + sC_TZ_1(1+sC_gR_{\mathrm{on}}) + sC_TR_{\mathrm{on}}(1+sC_{T2}Z_1)} \tag{A2}$$

TABLE I
ATTENUATOR MEASURED PERFORMANCE SUMMARY

	Kaunisto et al. [6]	Maoz [7]	This work
Technology	0.8 μm	GaAs	0.13 μm
Operation frequency	DC-900MHz	DC-8GHz	DC-2.5GHz
Minimum attenuation	3.3dB	2-3dB	0.9-3.5dB
Attenuation range	28 dB	14-15dB	42 dB
Return loss	>-12 dB (DC-0.9GHz)	Close to 50Ω	>-8.2 dB (DC-2.5GHz)
Insertion loss flatness	N/A	1dB	2.6dB (DC-2.5GHz)
Incremental Noise Fig.	<1dB	N/A	1dB per dB of attenuation
1dB compression point	5dBm	19dBm	2.5dBm
Supply voltage	2.75V	6V	1.2V
Power consumption	12mW	N/A	1.9mW

The attenuation of the network at low frequencies can be written as

$$\frac{1}{\text{Att}} = \frac{R_{M2}R_S}{R_{M1}R_S + R_{M2}R_S + R_{M1}R_{M2}}. \quad \text{(A6)}$$

Similarly, attenuation curve equations for a T-Network are

$$R_{\text{IN}} = \frac{R_{M1}^2 + 2R_{M1}R_{M3} + R_{M1}R_S + R_{M3}R_S}{R_{M1} + R_{M2} + R_S} = R_S \quad \text{(A7)}$$

$$R_{M1} = \sqrt{R_{M3}^2 + R_S^2} - R_{M3} \quad \text{(A8)}$$

$$\frac{1}{\text{Att}} = \frac{R_{M3}R_S}{R_{M1}^2 + R_{M1}R_S + R_{M3}R_S + 2R_{M1}R_{M3}} \quad \text{(A9)}$$

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