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A DC-2.5 GHz high linearity CMOS attenuator in a 0.18µm technology

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Abstract

A CMOS attenuator with high linearity has been designed and measured in a 0.18-µm CMOS process, to be used for a variable gain amplifier of RF wireless transceiver. The design is based on four cascaded Bridge-T attenuator stages that are consecutively activated to adjust the attenuation level and improve linearity. The design operates in the frequency band of DC-2.5 GHz with 2 - 3.5 dB insertion loss and 14 dB maximum attenuation in the entire frequency range. Measured and simulated results are in good agreement over the frequency band of interest. Measured worst case S11 and S22 are –10 and -8.8 dB, respectively, across the frequency band. The measured 1-dB compression point is +22 dBm at maximum-attenuation.

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Keywords: attenuator; digital attenuator; CMOS; linear-in-dB; linearity; wide bandwidth.

1. Introduction

The modern communication systems have the ability to control signal strength consistently in the signal path. The received power between the receiver and base station depending on the distance may vary by orders of magnitude. Hence, precise gain control circuitry is needed to limit the incident power to the receiver chain. Likewise, in the transmitter chain modern communication standards require stringent power control in the transmitting circuitry. For

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example, a CDMA phone needs adequate control of its output power in order to maintain an efficient link between the user and the base station [1].

The variable gain amplifiers (VGAs) have been the traditional choice in implementing variable gain elements. VGAs are not optimal for multi-band applications since they have narrow band performance. They also exhibit high power consumption and poor linearity such as, cable modem receivers where the incident power can be as high as 0 dBm in 75 Ω, the linearity and power handling requirements for the variable gain element can be extremely difficult to meet with active elements. Power dissipation in such amplifiers may be hundreds of milliwatts to meet the system specifications [2]- [4].

Passive resistor network and FET devices as switches can be used as digital-controlled variable attenuators with modest dynamic range and righteous matching. The low cost and availability of CMOS process make it an attractive choice of technology to integrate systems on a single chip. Furthermore, the downscaling of the CMOS technology continues to provide devices with higher f_T, which are suitable for broadband RF circuits. The purpose of this paper is to use the CMOS technology to implement a broadband multi-purpose attenuator, which can be integrated on chip in a system design. With the passive-type construction, the attenuator core has a wide bandwidth without penalties in power consumption [1], [2].

In this paper, a 4-bit CMOS digital step Bridge-T attenuator networks are demonstrated. Analysis of the proposed 4-bit attenuator is also studied. In section II, we discuss the circuit architecture of the attenuator. In section III, the design concept of the proposed topology and the analysis of the 4-bit attenuator are also explained. In section IV, the measured and simulated results of the attenuator circuit are presented; Conclusions are reported in section V.

2. Circuit Architecture

Several topologies of digital step attenuators, shown in Fig. 1, have been demonstrated in the literature [5] - [10] for switched Π/T attenuators. These attenuators mainly achieve relative attenuations from insertion loss differences by on/off control of R_F switches. The switched Π/T attenuators have series and shunt FET switches merged with a resistive network for attenuation. These topologies have a single series switch in a signal path. The parasitic difference of the switch on/off state, however, causes the transmission phase change.

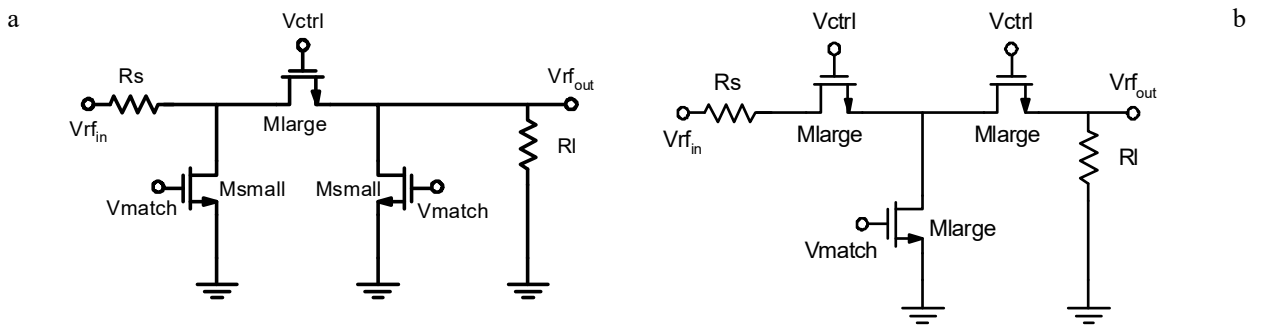


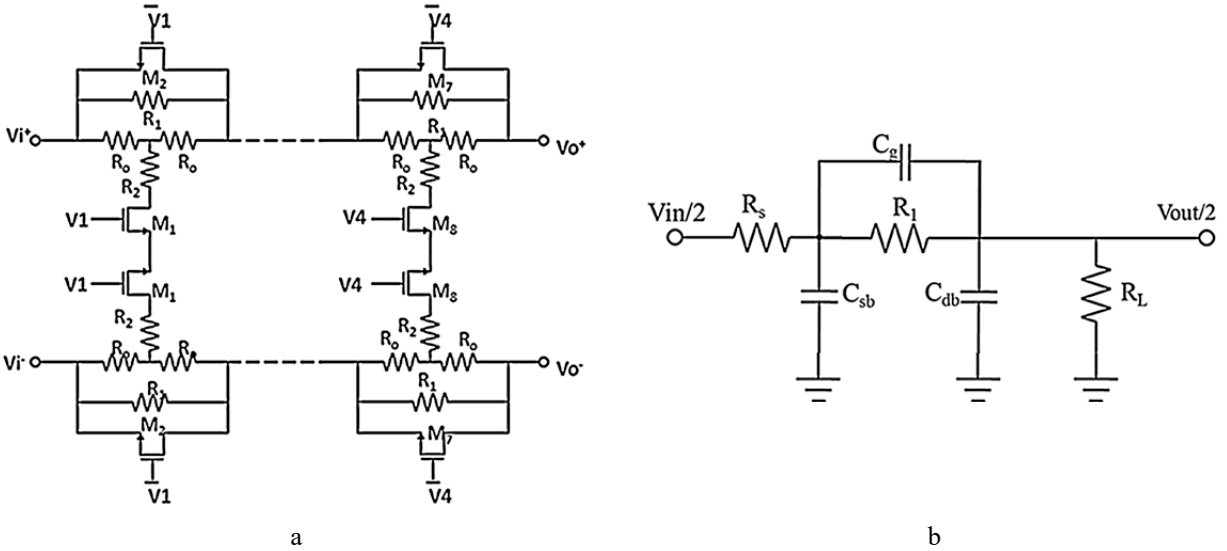
Fig. 1. Topologies of digital step attenuators Switched (a) Π and (b) T attenuators.

The Π-attenuator and T-attenuator shown in Fig. 1 are widely used as gain control elements. For linear-in-dB controllability, the series and shunt transistors are used as switches. A lot of efforts have been devoted to improve the linearity and matching of the discrete-step attenuator [4].

3. Circuit Design Approach

The schematic of the proposed differential attenuator is shown in Fig. 2-a. The proposed attenuator circuit consists of four cascaded bridge-T attenuators and utilizes different attenuation states controlled by 4-bit control

signal. The CMOS series and shunt transistors are sized to improve linearity and decrease the insertion loss (*IL*). They are used to switch between different attenuation levels.



a b

Fig. 2. (a) Four stages cascaded bridge-T attenuator, (b) The small signal model (half circuit).

The multi-stage bridge-T attenuator, shown in Fig. 2-a, includes four series resistor (R_1) with shunt NMOS transistors on the signal path and four shunt resistors (R_2) with series NMOS transistors connected from the signal path to ground. Typically, if the series NMOS transistors are turned off by an external control signal, the attenuator insertion loss is minimum which ensures proper impedance matching. On the other hand, if the series NMOS transistors are turned on, the shunt resistors will lead to maximum insertion loss with proper impedance matching. The value of the attenuation is determined by a combination of series-shunt resistances and parasitic capacitances, which is controlled by the bias signal across the NMOS transistors. The attenuator bit values are 1.5 (LSB), 3, 6, and 1.5 dB for a total attenuation of 12 dB. The four-bit control signal inputs (V_1-V_4), toggled between 1.8 and 0 V; are used to select each attenuation state. The output voltage V_{outRF} of the small-signal model for the single input/output attenuator is shown in Fig. 2-b when M_1 is turned on and M_2 is turned off. This stage is typically used to get the relationship between the Insertion Loss (*IL*) and the series resistance R_1.

The equation (1) of the insertion loss (*IL*) controlled by the series and shunt resistors R_1, R_2, respectively.

$$IL = \frac{1}{1+\frac{R_1}{R_S}} \frac{(1+sC_gR_1)}{1+s(C_g+C)R_1 \| R_S} \tag{1}$$

Where $Cg \approx Cgs/2$ and $C = Cdb = Csb$. For DC and low frequency, the series resistance R_1 in terms of *IL* will be,

$$R_1 = R_s(\mathcal{K} - 1) \tag{2}$$

By the same way for R_2, using the proper small signal model,

$$R_2 = \frac{R_S}{(\mathcal{K}-1)} \tag{3}$$

Where, *Rs* is the matching resistance and $\mathcal{K}$ is the DC attenuation factor.

4. Experimental and Simulation Results

The proposed digital-controlled variable attenuator has been designed, simulated, and measured using TSMC 0.18-µm CMOS technology. A photograph of the fabricated attenuator chip is shown in Fig. 3. The chip size is 125 µm × 208 µm, without pads. It was measured by on-wafer Cascade® probe station.

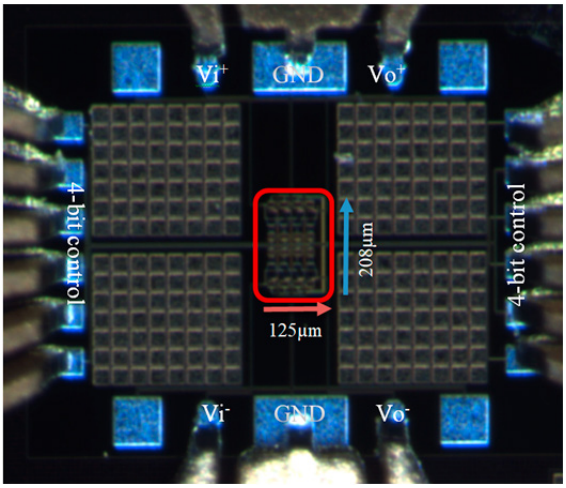


Fig. 3. Photograph of the fabricated attenuator.

Fig. 4 shows the measured insertion loss (S_{21}) as a function of frequency for minimum/maximum attenuation states. The minimum insertion loss of the through mode is 2.3 dB whereas the maximum isolation of the attenuation mode is 13.8 dB at 2 GHz.

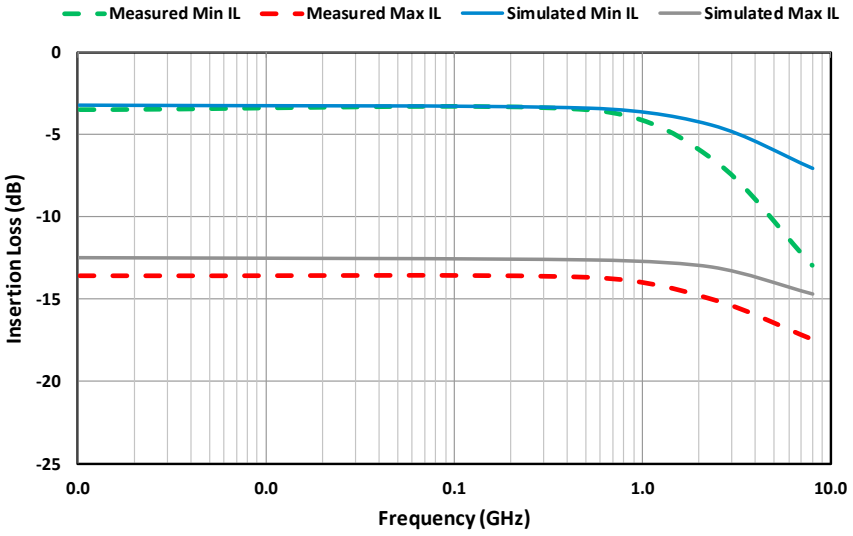


Fig. 4. Insertion loss vs. Frequency.

Fig. 5 shows, the insertion loss as a function of the attenuation states, it is approximately linear-in-dB at low frequency and cut off frequency. The upper 3-dB bandwidth is 2.5 GHz. The error of the attenuator is around ±0.5 dB with 1.5 dB steps.

The measured low frequency *IL* varies from -2.3 dB to -13.8 dB. The input 1-dB compression point was measured at maximum *IL*, as shown in Fig. 6, revealing a P1-dB of +22 dBm. (*IL*).

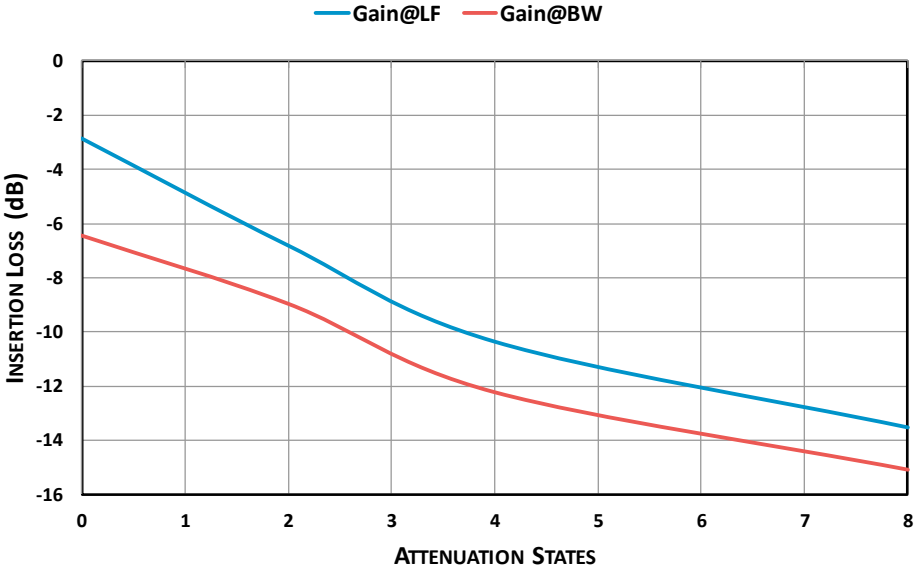


Fig. 5. IL Linear-in-dB vs. attenuation states.

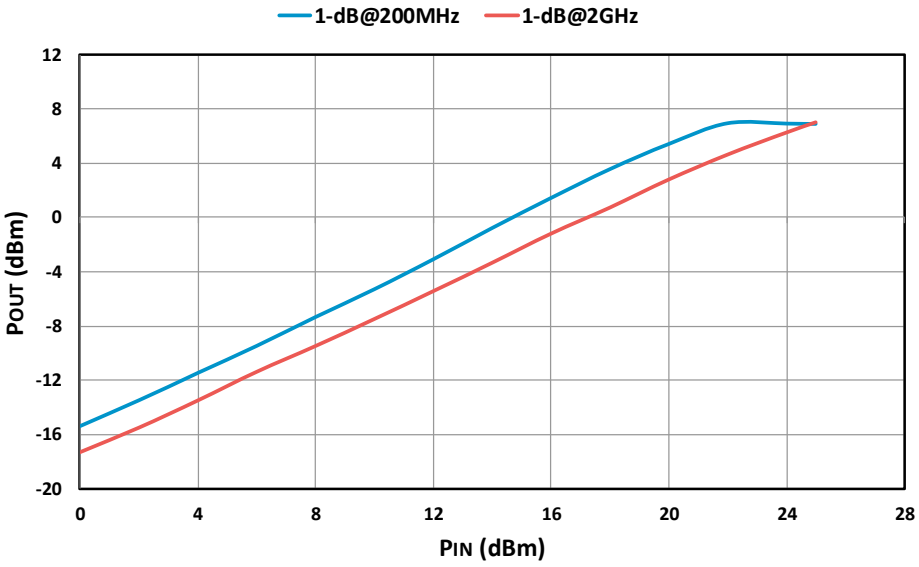


Fig. 6. Input P1-dB at different frequency.

Fig. 7 shows the measured input and output return loss (R_L) response of the proposed attenuator at different frequencies versus attenuation states settings. The worst-case vales of input/output return loss at low frequency are -10 dB and -8.8 dB, respectively. The measured performance of the proposed digital attenuator is reported and compared to previous work in Table I. The attenuator achieves a 12-dB dynamic range.

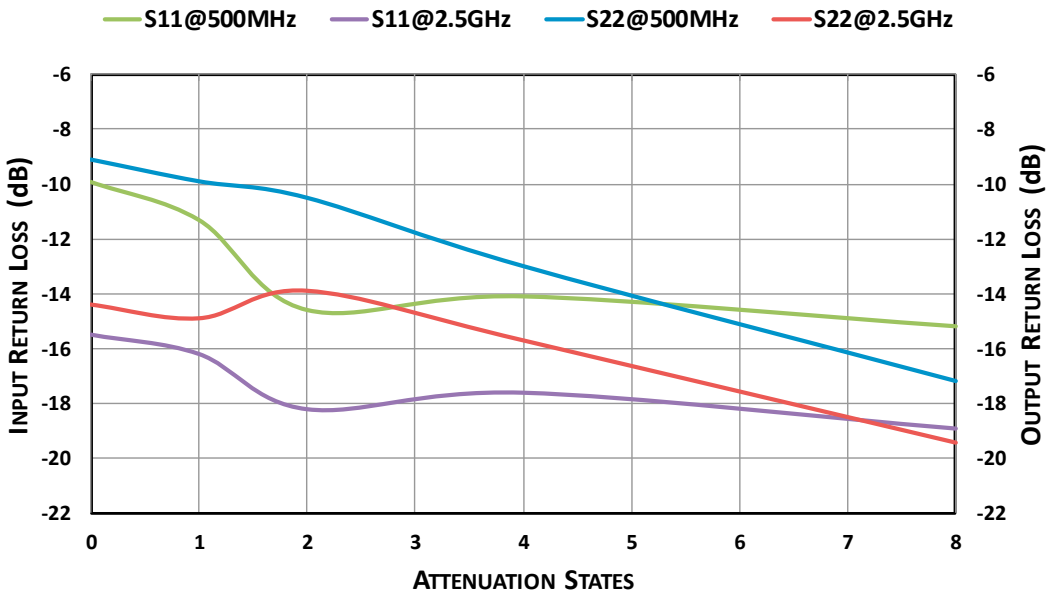


Fig. 7. Return loss vs. frequency at low and cut-off frequencies.

Table 1. Attenuator performance summary.

Parameters	[1]	[2]	This Work	Unit
Technology	0.13µm CMOS	0.18µm CMOS	0.18µm CMOS	-
Frequency	DC – 2.5	0.4 – 3.7	DC – 2.5	GHz
Attenuation range	42 (±)	33 (±1)	12 (±0.5)	dB
P_{1dB}	2.5	7.5	22	dBm
Input return loss	> -8.2	> -9	> -10	dB
Die area	700 × 1000	750 × 375	125 ×208	μm^2

5. Conclusion

In this paper, a high linearity digital attenuator with wide bandwidth was fabricated using 0.18-µm TSMC CMOS technology. The measurement at 2.5 GHz shows that the insertion loss is as low as 2.3 dB with a 22 dBm compression point in the through mode. The attenuation is digitally controlled over 12 dB by approximately 1.5 dB steps. The measurement results demonstrate that the designed attenuator can be effectively used for the variable gain amplifier of modern wireless transceivers and instrumentation system.

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