EECS 142 Laboratory #1

High Frequency Passive Components

Prof. A. M. Niknejad and Dr. Joel Dunsmore
University of California
Berkeley, CA 94720

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1 Introduction

Passive components play an important role in RF and microwave circuits. For instance, inductors are commonly employed to tune out the capacitance of transistors by forming resonant circuits. Inductors and capacitors together are used to build filters and impedance matching circuits. In communication circuits, filtering and matching are important functions for attenuating unwanted signals while maximizing the gain of desired frequencies. Unfortunately, there are no ideal inductors, capacitors, or resistors, and the unwanted characteristics of these components are called parasitics. In this laboratory, you will learn about the high frequency parasitics associated with passive components. These parasitics add loss and limit the upper frequency range over which the components function properly.

2 PCB Manufacturing

All circuits will be fabricated using a simple two-layer printed circuit board (PCB). The PCB consists of a low-cost dielectric material, usually FR4 ($\epsilon_r = 4.4$), with a thickness of 62 mils[1], and two layers of Cu metal layer. The copper layers are plated with solder, which doesn't oxidize and which melts at low temperature. The metal layers have a thickness of 34 μm. Normally you would pattern the metal layers to produce your circuit but in the interest of time, the boards have been prefabricated to take on a standard form. The backside of the board is a solid ground plane. Connections to ground must travel through a plated-through "via" to reach the backside.

A typical board used in later labs shown in Fig. 1. The input and output of the board have footprints for SMA connectors which allow you to connect SMA cables[2]. The input and output microstrip transmission lines are interrupted periodically which allow you to place components in series or in shunt. Landing pads with vias to ground also appear periodically to allow shunt components to be soldered to ground.

To solder components onto the board, use standard 0603 components[3] in series or in shunt. The components have lead-free solder plating (as all do, these days), so use lead-free solder. Also, use flux which is formulated specifically for lead-free soldering. See the ppt file on the class website for tips on precision soldering of 0603 lead-free components.

While Fig. 1 shows the amplifier board you'll use in Lab 3, the actual boards you'll be using in this lab are shown in Fig. 19 and Fig. 20. We'll make the assumption that the parasitics we characterize on the test boards in this lab, will be the same for the boards in, say, Lab 3. While this won't be completely true (FR4 material is low-cost with a large thickness tolerance so all boards might not have the same thickness). Nevertheless, we will make the assumption that however you characterize the parasitics in this lab, you can use those parasitic models for the boards used in later labs.

Another assumption we'll make is that the connectors' behavior is reproducible. The

[1] 1 mil = .001 inch = 25.4 μm

[2] SMA stands for SubMiniature version A, a connector for coaxial cables with 50Ω impedance and good performance up to 18GHz

[3] Components are classified according to their footprint size in mils, or in this case 0.060 inches by 0.030 inches.

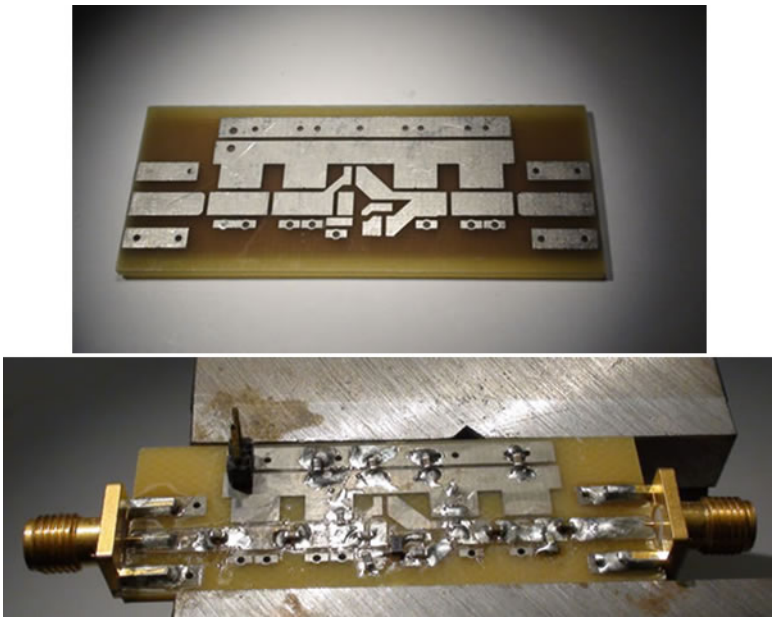

Figure 1: Top) Bare amplifier board to be used in Lab 3. Bottom) Stuffed version of the above board implementing a tuned amplifier for narrowband operation at 600 MHz. The point of this Lab 1 is to characterize the parasitics of these boards: the microstrip transmission lines (seen most clearly in the upper photo), and the gaps between transmission lines where you will solder components. You'll also characterize the intrinsic parasites of the 0603 components themselves. Whenever you use such components in later designs, you'll need to account for both the 0603's intrinsic parasitics and the 0603's extrinsic parasitics which arise from how it's mounted onto the board - so that you can design high-frequency circuits in later labs that will work correctly as designed

term "repeatable" is used to mean the behavior is the same when we connect and remove one connector from the same mating connector. The term "reproducible" is used to mean that the SMA connectors you have on your Lab 1 boards will behave the same as the SMA connectors on your Lab 3 board. Connectors have tolerances also, so they can't behave identically, but we'll assume they do. Just be aware of what assumptions are buried in these labs.

One thing we won't assume, is that the designer of these boards was successful in creating 50 ohm transmission lines. It's always possible that a panel gets over-etched or under-etched, so that the traces come out wider or skinnier than the designer specified. You'll characterize the transmission line of a "Thru" board in this Lab 1 (on a per-length basis) and then use whatever model you find, for subsequent labs' transmission lines. That is, we'll assume that the Thru board's transmission line's characteristic impedance might be something other than 50 ohms, but whatever we measure it to be, we'll use that per-unit-length transmission line model when designing the Lab 2 bandpass filter and the Lab 3 amplifier.

In these labs, we'll combine the above assumptions with two measurement techniques: 1) calibrating to the ends of the cables in a first-tier calibration, followed by 2) using Port Extension all the way to the 0603 component's leads (as a second-tier calibration), to derive models of parasitics. This strategy for characterizing parasitics should lead to successful circuits in the subsequent labs.

If you're interested in more advanced techniques that RF engineers use (de-embedding, etc.), there might be time at the end of the course to discuss those.

3 Lumped Passive Components

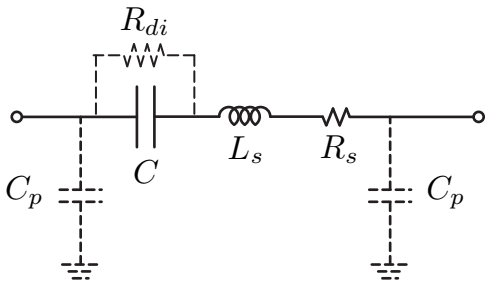

Figure 2: The lumped equivalent circuit model for a real soldered capacitor.

Up to now you have probably simulated your circuits with ideal passive components (inductors, capacitors, resistors), but real circuit components are far from ideal. Consider, for instance, a capacitor, which has an equivalent circuit model shown in Fig. 2. The model has many parasitic components which only become relevant at high frequencies. A plot of the impedance of the capacitor, shown in Fig. 3, shows that in addition to the ideal behavior, the most notable difference is the self-resonance that occurs for any real capacitor. The self-resonance is inevitable for any real capacitor due to the fact that as AC currents flow through a capacitor, a magnetic field is also generated by the capacitor, which leads to inductance

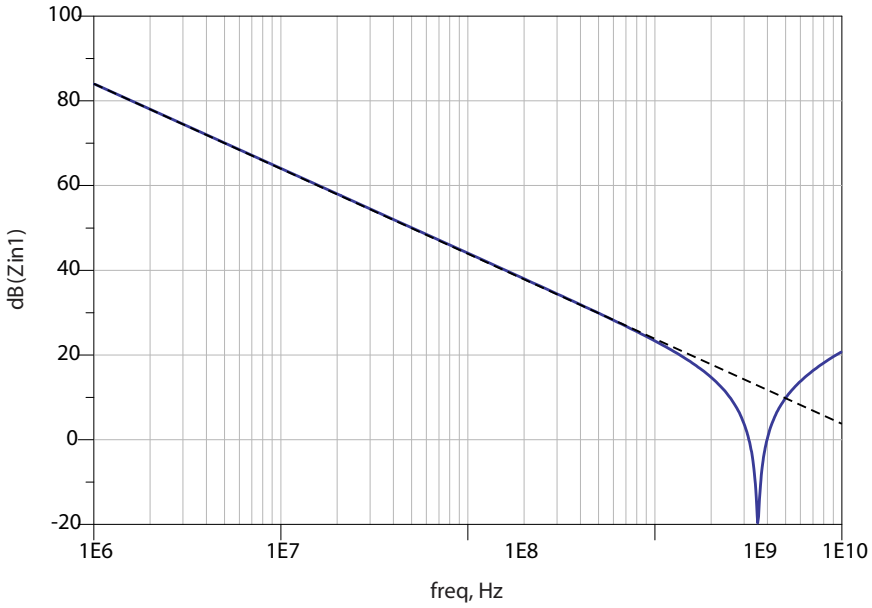

Figure 3: The magnitude of the impedance of a real capacitor (the dashed line shows the ideal behavior).

in the structure. This inductance is exacerbated by the leads of the capacitor, which often dominate the inductance. The inductive parasitics are lumped into a single inductor L_s in series with the capacitor. The finite conductivity of the plates and the leads also results in some series loss, modeled by R_s (sometimes labeled ESR, or effective series resistance). Unless a capacitor is fabricated in a vacuum, the dielectric material that separates the plates also has loss (and resonance), which is usually modeled by a large shunt resistance, R_{di}. Furthermore, when a capacitor is soldered onto a PCB, there is parasitic capacitance from the solder pads to the ground plane, resulting in the capacitors, C_p, in the equivalent model.

In a like manner, every inductor also has parasitics, as shown in the equivalent circuit model (Fig. 4), which limit operating frequency range. The series resistance, R_x, is due to the

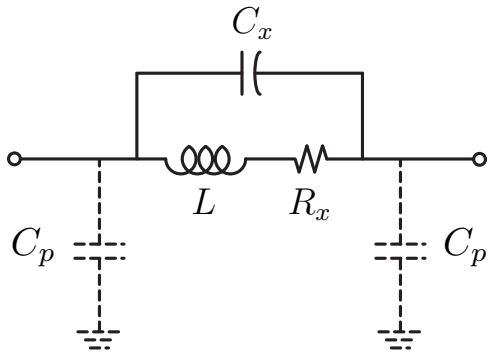

Figure 4: The lumped equivalent circuit model for a real soldered inductor.

winding resistance, and the capacitance C_x models the distributed turn-to-turn capacitance of the windings. The inductorself resonates at a frequency of approximately $1/\sqrt{LC_x}$ and has a quality factor $Q = \omega L/R_x$. When the inductor is soldered onto the PCB, there is an additional capacitance to ground modeled by C_p, which lowers the self-resonant frequency to $1/\sqrt{L(C_x + C_p/2)}$.

4 Board Parasitics

In addition to the component parasitics, you will find that there are significant parasitics associated with the PCB. When you solder a component in series between two microstrip traces on a board, the placement of the component relative to the ground plane will affect the inductance and capacitance of the component. Likewise, when you solder a component to ground, the via path will affect the inductance. There is both inductance and resistance associated with the via to the ground plane.

Traces between components act as transmission lines and can therefore be modeled as LC circuits at low frequencies if the length of the trace is much shorter than the wavelength ($\ell \ll \lambda$). For example, ideally a short circuit should have zero impedance, but as the measurements will show, there is a finite amount of inductance and resistance below the self-resonant frequency.

It is important to realize that the ground plane itself contributes resistance, especially at higher frequencies when the current flow is non-uniform and flows directly underneath the top trace of a microstrip transmission line. As explained in more detail in the next section, the "inductance" of the components is strongly related to the "return current", or the path of the current flow under the component. If the ground path beneath the component is interrupted, forcing the current to flow away from the component, the parasitic inductance increases considerably.

4.1 Component Specifications

Inductors and capacitors are often described in terms of the (1) inductance/capacitance at a particular frequency, (2) quality factor and (3) self-resonant frequency (SRF). The inductance/capacitance varies due to the non-ideal behavior of the component. For instance, the intrinsic inductance may vary with frequency due to non-uniform current flow (current crowding) at high frequencies. More prominently, though, the inductance/capacitance varies due to the complex parasitics associated with the component. Instead of specifying the equivalent circuit model, many manufacturers simply specify these two or three numbers. If the components are used well below their self-resonant frequency, these three numbers may be sufficient to characterize the structure.

The quality factor, Q, is very important in RF circuits, since it ultimately limits the performance of amplifiers, filters, and other circuits. At frequencies well below resonance, the Q factor is given by

$$Q = \frac{|X_{L|C}|}{R_x}$$

where $X_{L|C}$ is the reactance of the component at a given frequency and R_x is the effective

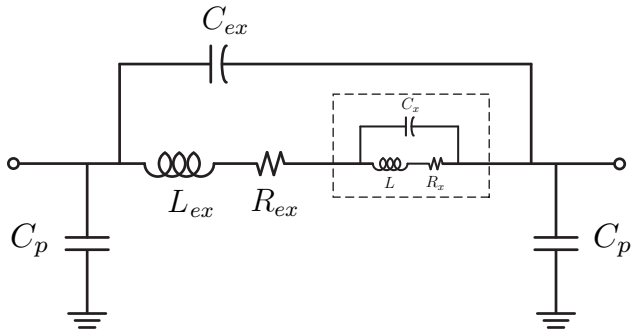

Figure 5: The lumped equivalent circuit model for an inductor includes *extrinsic* and *intrinsic* parasitic components.

series resistance (ESR) of the component. In fact, instead of Q, the ESR may be given. It's important to note that Q is a function of frequency.

The self-resonance is determined by the parasitics in the structure, and when a manufacturer of a component specifies this value, it's difficult to know what they mean! For instance, for a capacitor, the series inductance is a strong function of how the component is connected to the board. The consequent geometry will set the parasitic inductance and hence the self-resonant frequency. One can only guess how the component was characterized. For instance, if an 0603 capacitor is measured as a two-port circuit using transmission line interconnect, then inductance is a strong function of the characteristic impedance of the line's Z_0 (see below). It is therefore advisable to measure the self-resonance frequency of the component for the application at hand by measuring test structures on test boards which have similar geometry to what you'll use in your final design. RF designers often send out boards with such structures before they fab their final board designs. This way, parasitics can be characterized on the test boards, and their effects compensated for in the final design.

4.2 The Origin of Component Parasitics

As we discussed, the parasitics of a non-ideal inductor shown in Fig. 4 include series loss R_x, a "winding" capacitance C_x, and parasitic capacitance C_p. These parasitics arise from two sources: (1) intrinsic parasitics related to the way the inductor itself is physically constructed and (2) extrinsic parasitics resulting from the way the component is soldered on the PCB substrate. In the case of integrated circuit (IC) inductors, the same parasitics arise, but the extrinsic parasitics are related to the Si substrate as opposed to the PCB substrate. In Fig. 5, we divide the equivalent circuit into the intrinsic and extrinsic portion.

The intrinsic losses can be understood by examining a typical solenoidal air-core inductor used for RF applications (Fig. 6). Since the winding wire has resistance, the inductor winding must include a series resistance, R_x, in the equivalent circuit model introduced in Fig. 4. Likewise, since the windings of the inductor come in close proximity, at very high frequencies signals can skip the loop and travel directly from winding to winding through the intrinsic capacitance between the windings. This is especially true at high frequencies when the potential difference between the windings increases ($V_{diff} \propto \omega L_w$). The effect of

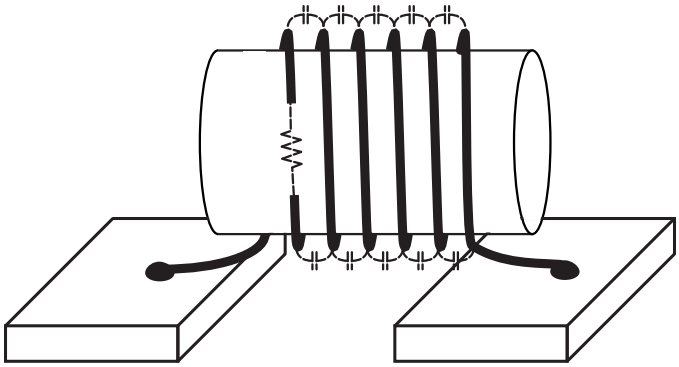

Figure 6: A solenoidal "air-core" high frequency inductor geometry.

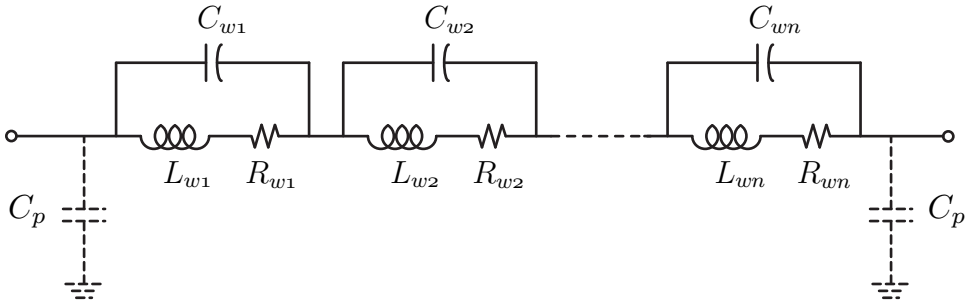

Figure 7: Distributed model for a solenoidal inductor.

the interwinding capacitance is modeled by the capacitor C_x in the equivalent circuit model.

In reality, the interwinding capacitance is distributed non-uniformly throughout the structure and a more sophisticated model, shown in Fig. 7, can be used to capture the impedance of the structure more accurately. In practice, though, this is not necessary as long as we employ the inductor well below its *self-resonant frequency* (SRF), ω_0. The SRF is defined as the frequency at which the imaginary portion of the inductor impedance $Z_L(\omega_0)$ reaches zero, $\Im\left(Z_L(\omega_0)\right) = 0$. Above this frequency the inductor begins to behave like a capacitor, as more energy is stored in the electric field rather than the magnetic field. This occurs because the signal is bypassing the windings in favor of the capacitive coupling mechanism (i.e. the interwinding capacitance).

When an inductor is used in any real circuit, it must be connected to other components through traces on the PCB, as shown in Fig. 8. Here we see that pads on the PCB are used to form the correct footprint for the inductor so that it's possible to solder the leads of the inductor to the PCB substrate. If we define the outer edges of where the inductors' leads align with the outer edges of the pads, as locations A and B, we can clearly see that capacitors C_p are needed to model the pads' capacitance to the substrate, since the back-side of the substrate is usually a ground plane.

There is a gap on the PCB between the inner edges of the pads. These locations are marked C and D in Fig. 8. A small electrical fringing field can couple across this gap as shown in Fig. 9. The presence of the ground plane greatly reduces this coupling capacitor

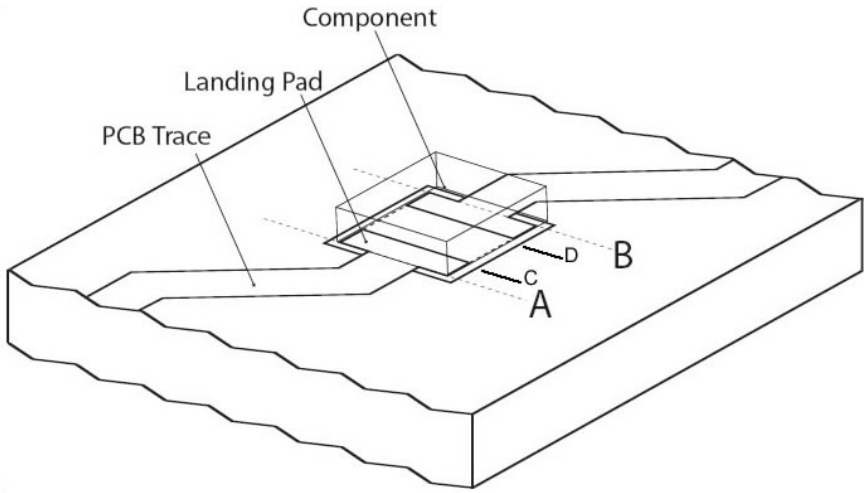

Figure 8: The footprint of an inductor on a PCB substrate consists of two landing pads. PCB traces connect each pad to other components on the board. The 0603 device which we solder onto the board has leads, which are the two metalized ends that sit on the footprint's pads. The bottom side of the board is a solid ground plane.

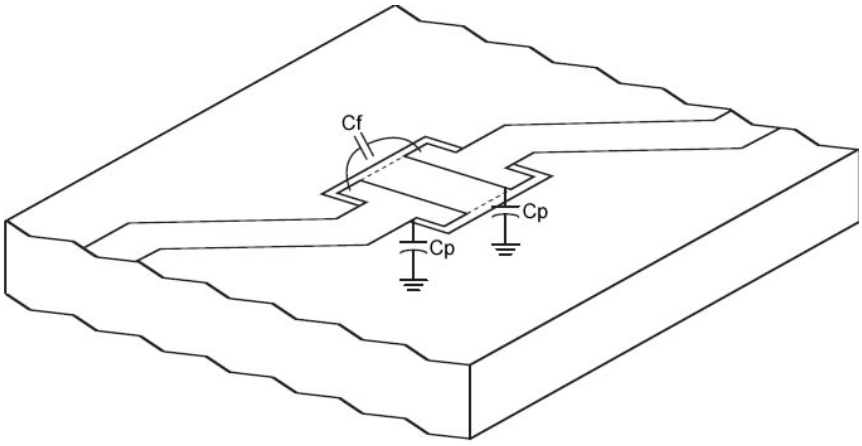

Figure 9: The capacitance between the landing pads includes a coupling capacitor due to the fringing fields between the pads.

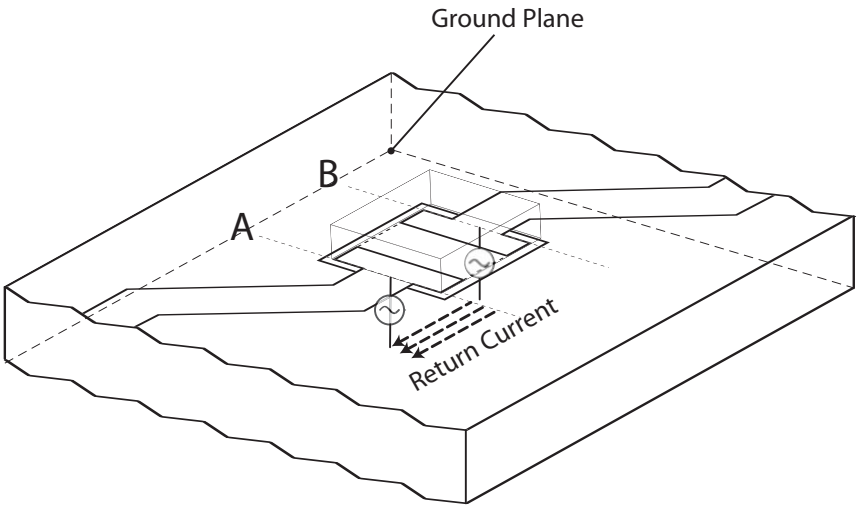

Figure 10: The return current in a PCB inductor flows through the ground plane.

C_f, but as components are reduced in physical size or if the substrate thickness is made larger, this coupling increases.

While an 0603 component's pad capacitors are easy to understand, the concept of lead inductance is much more difficult to explain. Recall that the inductance of any structure is only defined for a *closed* loop. Since the reference lines A and B are physically separated, the inductance between them must include a "return path" for the current. Imagine connecting voltage sources at locations A and B as shown in Fig. 10. Now we can see that current flows in a loop by flowing through the ground plane between A and B. This loop stores magnetic energy and thus has an inductance L_{ex}, which we incorporate into the equivalent circuit model of Fig. 5. It is important to realize that to first order, this lead inductance is independent of the inductance of the component inductor since the current flows through the same path regardless of the value of inductance L. In fact, if we short out the gap between A and B, we still experience the lead inductance L_{ex}. We therefore augment the equivalent circuit model to account for this extra *extrinsic* inductance in the component, which is a function of the layout of the component rather than the component itself. Since traces on the PCB also incur additional loss, an extra resistance, R_{ex}, has been added to the model as well.

For integrated circuits, the same considerations apply with a couple of small minor adjustments. A typical integrated inductor is made in spiral form, as shown in Fig. 11. Inter-winding resistance and coupling capacitance occur as well, but the substrate is usually quite thick compared to the dimensions of the spiral. Typically, the substrate is $700\mu m$ thick. The back of the substrate is not always an ideal ground plane (sometimes a non-conductive glue is used to attach the die to the package) and the return-current signal path is actually just below the surface of the substrate through metal layers. Since these return-current layers can be made very close to the top-metal inductor windings, the extrinsic inductance can be reduced significantly. In Fig. 12, the windings are routed in such a manner as to close the loop, effectively producing a one-port structure. The most important complication for inte-

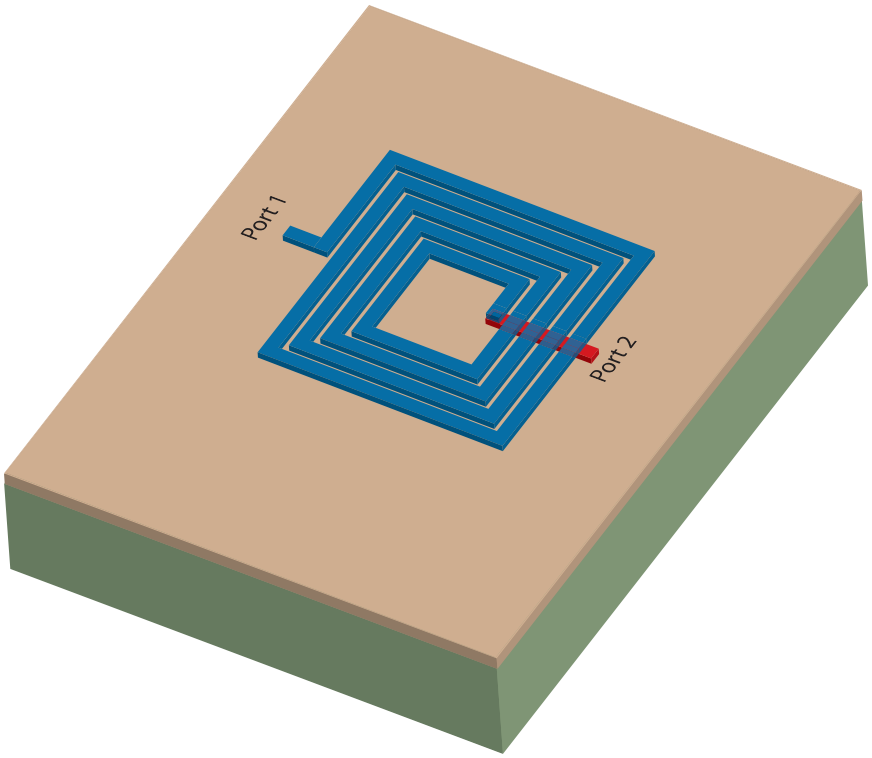

Figure 11: The layout of an on-chip spiral inductor (two-port structure, with the ground connection for each port being either the substrate of a deposited metal layer just below the top-metal layer).

grated inductors, though, arises from the capacitive coupling through a doped Si substrate (conductivity varies but a good typical value for a modern process is about 10 Ωcm), which is modeled by including series resistances, R_{sub1} and R_{sub2}, in the equivalent circuit model shown in Fig. 13. It is important to note that depending on the thickness and conductivity of the substrate, the coupling between the end leads of the inductor, through the substrate, varies significantly. An extra resistance, R_{sub3}, models the coupling through the substrate. The extra substrate capacitors, C_{sub1} and C_{sub2}, model the displacement current flow in the substrate.

It is now easy to see that all the (extrinsic and intrinsic) inductance can be lumped into a single inductor L, in Fig. 4, while all the resistance is lumped into R_x. This simpler model shown in Fig. 4 is thus adequate for capturing the high frequency behavior of the component if it is employed well below the self-resonant frequency. Near or above the SRF, the component is dominated by distributed behavior and a simple lumped circuit such as this one cannot capture the behavior.

It is now clear that other components besides inductors can be similarly divided into intrinsic and extrinsic parasitics. For instance, a large discrete capacitor is physically manufactured by sandwiching several plates and stacking or rolling the plates to realize a large capacitance in a small volume (Fig. 14). For RF applications, many capacitors are made by using a flat parallel plate structure called a metal-insulator-metal (MIM) capacitor. A very

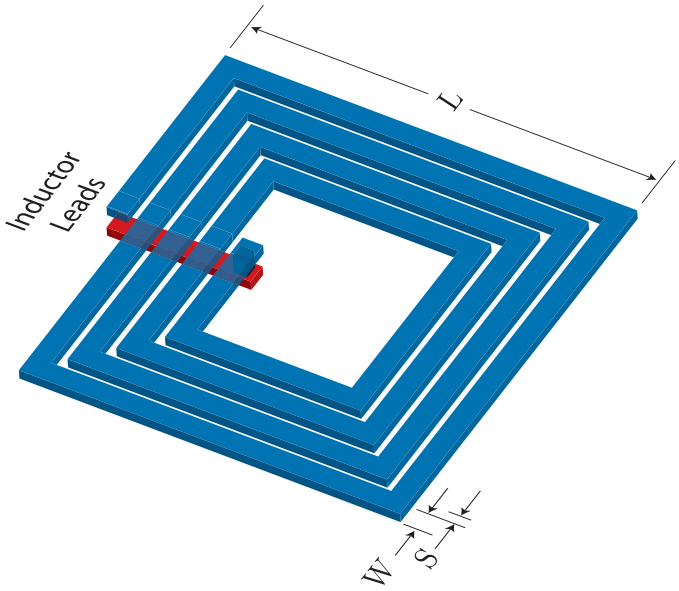

Figure 12: The layout of an on-chip spiral inductor (one-port structure, where the port is across the two ends of this winding).

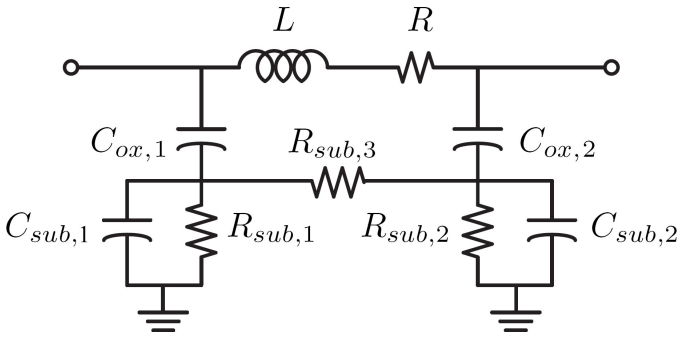

Figure 13: The model for an on-chip inductor on a lossy substrate.

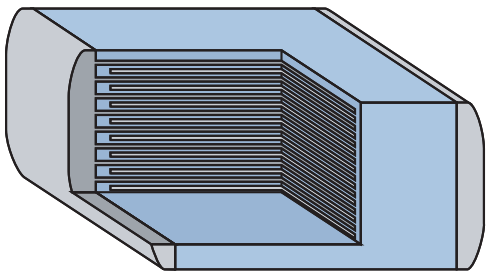

Figure 14: The physical layout of a multi-layer surface-mount capacitor. (Source: Wikipedia)

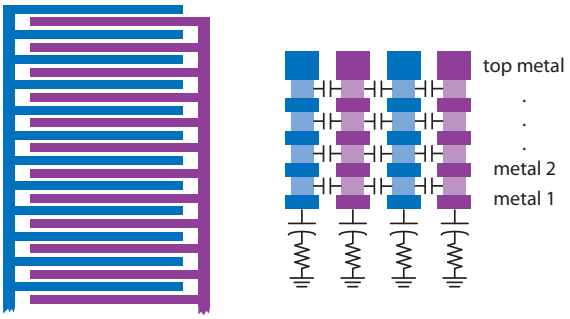

Figure 15: A MIM "finger" capacitor layout.

thin insulator is used to maximize the capacitance between the plates. In an IC process, lateral or flux capacitors use small interdigitated fingers to realize a high capacitance between the end leads of the capacitor (Fig. 15). Due the materials employed in the construction of the capacitor, we model the lead series resistance as R_s in Fig. 2. The parasitic inductance, L_s, of the capacitor is due to the magnetic energy storage in the structure when we connect a voltage source between the leads and measure the AC current flow. At high frequencies, we find that the reactive portion of the impedance increases and crosses zero at the self-resonant frequency. This behavior is modeled by the capacitor's series inductance, L_s. The value of L_s is very dependent on how we connect the capacitor's leads to other components. If the capacitor is placed on a PCB substrate, then its parasitic lead inductance is defined by the return current loop formed by the ground plane as shown in Fig. 10. As before, we account for the pad capacitances by adding capacitors, C_p, to the model.

4.3 Calculation of Component Parasitics

It is useful to estimate the parasitics of a component by using some simple assumptions. A very common layout technique in RF PCB circuits is the microstrip configuration shown in Fig. 16. Fig. 16 shows just the trace portion of the layout of Fig. 8.

Fig. 8 shows both the traces and a component footprint. There, the leads of the component would be soldered to the component's "landing pads" (which are large enough for the component to fit), which may be wider than the traces used for interconnect. If we assume that the current flows across the landing pads and through the component in the direction of the trace, and assuming there is a ground plane underneath the structure, we can model the component's parasitics as a transmission line of length ℓ, propagation constant γ, and characteristic impedance Z_{TL}. That is, even if the component is a zero ohm resistor, the mere presence of its finite-geometry footprint needs to be accounted for, and we can account for it by modeling it as a transmission line (i.e. by Z_{TL}, γ and ℓ, or equivalently by the C-L-R-C model of Fig. 17).

For any given microstrip transmission line, the characteristic impedance, Z_{TL}, can be calculated using standard tables or approximate equations (online tools are also available) once the the width and height of the microstrip line are specified. From transmission line theory, the equivalent circuit for a short section of transmission line $\ell \ll \lambda$ is given by Fig. 17,

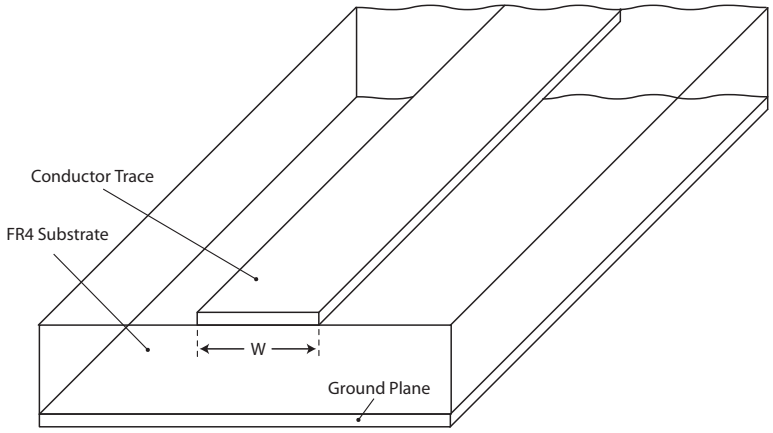

Figure 16: A microstrip transmission line formed on a PCB substrate.

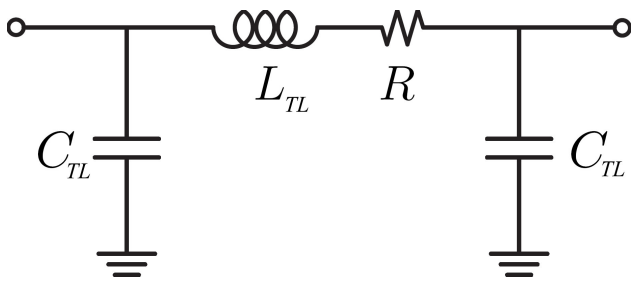

Figure 17: An equivalent circuit for a short section of a lossy transmission line, such as a microstrip line on FR4.

where λ is the quasi-TE mode propagation wavelength in the PCB. If the dielectric constant of the PCB is much larger than the dielectric constant of air, then the wave propagates mostly in the PCB medium, with a velocity $v = c/\sqrt{\epsilon_{re}}$, where ϵ_{re} is the effective relative dielectric constant for microstrip geometry. More accurate values of v can be obtained from approximate equations or tables.

The modeling component values for a transmission line for the Fig. 17 model (ignoring loss) are calculated as follows

$$\omega L_{TL} \approx Z_{TL}\beta\ell = Z_{TL}2\pi\frac{\ell}{\lambda}$$

$$\omega C_{TL} \approx \frac{1}{2}Y_{TL}\beta\ell = Y_{TL}\pi\frac{\ell}{\lambda}$$

Here, for a lossless model, we've assumed that the attenuation constant, α, in the expression for the complex propagation constant, $\gamma = \alpha + j\beta$, is zero.

At 1 GHz, the wavelength in free-space is 30 cm, and in the PCB it's 15 cm. That is, since the relative dielectric constant of FR4 is about 4, the velocity of the wave in the FR4 transmission line will be $1/sqrt(4)$ of the velocity of light in vacuum, or half of 3×10^8 m/s. An 0603 component is 60 mils long (and 30 mils wide), or about 1.5 mm long, which is only 1% of the wavelength. Therefore, our lumped circuit model for the transmission line will be reasonably accurate. Assuming $Z_{TL} = 50\Omega$, then the inductance is approximately given by $L_{TL} = 0.5$ nH. Typically, the landing pads of a footprint are designed to extend a bit beyond the length of the 0603 part so that a solder fillet has room to make a toe on each end of the component. As an estimate, let's assume the pads make the overall footprint be 120 mils by 30 mils (i.e. twice as long as the 0603 part itself). In this case, the modeling inductance is double what we just calculated, or about 1 nH. The modeling capacitance is $C_{TL} = 1$ fF. With this method then, we can model the parasitics due to the space that the 0603 component takes up on the board (i.e. the 120 mil by 30 mil footprint). This calculation has assumed that that component and its pads were wider than the trace width (as shown in the earlier figures), which holds for 0603 parts when the substrate is very thin. Our boards are rather thick and the 0603 components are actually skinnier than the trace width so you would modify the modeling steps accordingly.

If the length of the transmission line approaches a significant fraction of the wavelength, then a more accurate model of a component's parasitics can be employed. The Y parameters of the transmission line are given by

$$Y_{11} = Y_{22} = Y_o \coth(\gamma\ell)$$

$$Y_{12} = Y_{21} = -Y_0 \mathrm{csch}(\gamma\ell)$$

where $\gamma = \alpha + j\beta$ is the complex propagation constant (including loss). The complex hyperbolic functions can be calculated by

$$\coth(\gamma\ell) = \frac{\cosh(\alpha\ell)\cos(\beta\ell) + j\sinh(\alpha\ell)\sin(\beta\ell)}{\sinh(\alpha\ell)\cos(\beta\ell) + j\cosh(\alpha\ell)\sin(\beta\ell)}$$

$$\mathrm{csch}(\gamma\ell) = \frac{1}{\sinh(\gamma\ell)} = \frac{1}{\sinh(\alpha\ell)\cos(\beta\ell) + j\cosh(\alpha\ell)\sin(\beta\ell)}$$

Figure 18: A network analyzer (Agilent E5071C ENA RF network analyzer).

5 The Network Analyzer

In this class, you'll make extensive use of a network analyzer. A typical network analyzer is shown in Fig. 18. This instrument is also called a VNA, or Vector Network Analyzer, to emphasize the complex nature of the measurements (as opposed to scalar). That is, a VNA measures both magnitude and phase of a signal, whereas older scalar analyzers only measured magnitude.

Simply stated, a network analyzer measures the N-port response of a circuit over a specified frequency range. Most network analyzers are designed to measure two-port devices, since most filters, amplifiers, and other RF building blocks are two-ports. If only 1 port is used, then the network analyzer can measure the 1-port response, or the impedance of the device under test.

Network analyzers incorporate directional couplers to decompose the voltages seen at each port into "incident" and "reflected" waves. The ratio between these waves is directly related to the scattering, or S-parameters, of the device. Inherently, therefore, the network analyzer measures the S-parameters of the device under test. The S- parameters are easily converted into other parameter sets, such as impedance (Z) or admittance ($Y = Z^{-1}$) parameters.

The measurements made by a network analyzer can be saved and exported in SNP file format, where N is the number of ports used in the measurement. Typically you will be saving S2P files. The S2P file is an ASCII file format that is easy to read and import into other programs. Most CAD tools such as Agilent's ADS, or Cadence's SpectreRF or AWR's Microwave Office, or Mathworks' Matlab RF Toolbox, can read these S2P files. Matlab's RF Toolbox has built-in functions which simplify converting the S2P files you save from your network analyzer, to the corresponding vector (across the frequency sweep) of Y or Z parameters.

In this lab, you will be estimating the parasitics of 0603 components and our PCBs, by using the "port extension" feature of the Agilent network analyzer. The port extension

(a) (b)

Figure 19: (a) Open board to be used with either the manual or automatic port extension feature of the network analyzer. (b) ShuntShort board to be used for characterizing the via to ground.

feature enables you to move the reference plane from the tips of your SMA cables' connectors to the gap on the PCB where the your 0603 device is connected.

To utilize this port extension feature of the network analyzer, you will need to measure an "Open" board as shown in Fig. 19a. Make sure to include the loss in your measurements. This loss-modeling feature is a sub-selection under the Port Extension menu on the analyzer. The network analyzer will then automatically calculate the phase delay and loss associated with the traces forming the microstrip transmission lines on the board. This effectively moves the reference planes for Ports 1 and 2, for zero phase and zero loss, to the edges of the gap. Subsequent measurements are then reported with respect to this new pair of reference planes.

You will then use measurements of the ShuntShort board shown in Fig. 19b to isolate the location of the via and characterize it for its parasitic inductance. With the information gleaned from these first measurements of the Open and ShuntShort boards, you can understand the effects of the gap's fringing capacitance and the via's inductance.

Next, you'll measure the parasitics of a component in series or in shunt using the test boards shown in Fig. 20. For instance, you can measure the two-port parameters of a zero-ohm resistor when in series or shunt with the signal path.

The shunt components need to be characterized separately from the effects of the via to ground. Using the parasitics of a zero-ohm resistor allows you to to estimate the effect of the component parasitics due to the board layout. Alternatively, you can also measure the actual performance of the lumped components (inductors, capacitors) and model the component loss and resonance with an appropriate equivalent circuit.

Before performing measurements using a VNA, use the pin-depth gages to make sure your cables are within spec. Then you need to calibrate the instrument. This is needed since the internal directional couplers are non-ideal. Calibration also allows you to move the reference plane of the measurement to the tips of the cables. Manual calibration involves connecting a set of calibration standards to the VNA (opens, shorts, thrus, loads, etc.) step by step. An ECal is an electronic calibration instrument which has all the standards built in. It connects to the VNA over a USB bus and the VNA will automatically perform the calibration in one step.

After any calibration, always verify that the cal was good by measuring some standard other than the ones used in the calibration, and compare the measurement to its model. Refer

(a) (b)

Figure 20: DUT boards that 0603 devices can be soldered to. (a) The Open board allows a component to be soldered in series and characterized. (b) Shunt components can be soldered to ground on this board for characterizing components soldered in this configuration (the same physical 0603 component used in series or in shunt, will have different models). In each case, a zero ohm resistor can be used to estimate the series/shunt inductance.

back to Lab 0 and the Calibration.ppt file on the lab resources web site. To get consistent and accurate results, always use the torque wrench and a separate open-end wrench to connect the cables to the VNA and to the board.

6 Prelab

Review the ppt files on the course web site covering precision soldering and network analyzer calibration. There is also an introductory video tutorial by Dr. Dunsmore on using the network analyzer, from when the equipment was first donated in 2007. There is a copy of his book, Handbook of Microwave Component Measurements, in the Cory 111 lab and it is also available on the library website. Skim through it. Also watch his video (posted on the course web site) from his visit of Nov 2012, where he specifically goes through this lab and explains what the measurements and models should look like.

In the post-lab, you'll use ADS, Microwave Office or Matlab's RF Toolbox to read in the S2P files from your measurements. Review the tutorial cheat sheets on whichever tool you choose, and make sure you understand how to drive the CAD tool flow.

1. Calculate the impedance of a lumped inductor modeled by Fig. 4. Plot the impedance with component values: $L = 5$ nH, $R_x = 1.15\Omega$, $C_p = 400$ fF, $C_x = 10$ fF.

   (a) Compare the impedance to an ideal inductor by overlaying their plots on a log scale for the y-axis (in dB). Leave the frequency axis as a linear scale. Also plot the effective inductance of the structure ($\Im(Z_{ind})/\omega$) as a function of frequency.

   (b) Over what frequency range does the inductor behavior appear close to ideal behavior?

   (c) What is the self-resonant frequency (SRF) of the inductor? You can calculate the SRF using the simplified equivalent LC circuit.

   (d) What is the effective inductance near resonance? After the self-resonance frequency, how would you describe the inductor behavior?

(e) Over what range of frequency is the inductor a high Q component?

(f) Plot S_{11} of the inductor on a Smith Chart from DC to 10 GHz. Also, plot S_{21} on a LogMag plot. Vary the component parasitics using the tuning feature of the CAD tool and observe the behavior on the Smith Chart. Make sure you qualitatively understand each plot. You should get an intuitive understanding of the relative importance of each of the parasitics. Note that the equivalent inductance tends to infinity at the SRF. Below the SRF, the inductance can appear much larger than the nominal value (and often it is in this region of frequency that an inductor is used). The other aspect to note is that above the SRF, the inductor looks essentially like a capacitor.

2. Suppose that the inductor model in the previous section is actually an air-core inductor made of 5 windings. Simulate a distributed model of the inductor by assuming that the L and C_p are uniformly distributed from turn-to-turn. Compare the frequency dependent impedance of the distributed model with the simple model. Over what frequency range is the simpler model adequate? (This question might not be stated as intended, as it doesn't match Figure 7 on page 7. That figure has C_w and R_w distributed across turns, not C_p. But I guess it's possible that L and C_p might be what's intended here (?). C_p could be distributed, as the bottom edge of each turn will also have some parasitic capacitance to the ground plane.)

3. Calculate the impedance of a lumped capacitor modeled by Fig. 2. Plot the impedance with component values: $C = 5$ pF, $R_x = 0.25\Omega$, $L_s = 0.75$ nF, $C_p = 20$ fF.

   (a) Compare the impedance to an ideal capacitor by overlaying their plots on a log scale for the y-axis (in dB), linear scale for the frequency axis.

   (b) Over what frequency range does the capacitor behavior appear close to ideal behavior? Plot the effective capacitance seen from terminal to terminal and compare to the low frequency value. Up to what frequency can you employ this capacitor if you cannot tolerate a deviation by more than 10%?

   (c) What is the self-resonant frequency of the capacitor? What is the effective value of capacitance very close to resonance?

   (d) Over what range of frequency is the capacitor a high Q component?

   (e) Plot S_{11} of the capacitor on a Smith Chart from DC to 10 GHz, and plot S_{21} on a LogMag plot. Vary the component parasitics and observe the behavior on the Smith Chart. Make sure you qualitatively understand each plot.

7 Experimental Work

7.1 Procedure

1. The first step is to carefully and correctly calibrate the network analyzer and your cables. The process of calibration will move the reference plane to the tips of the

cables assuming you don't move the cables (much) during calibration or afterwards. The more phase stable a cable is, the more it can tolerate motion without compromising the error-correction that was performed on it during calibration.

You can perform the calibration with the E-Cal or with mechanical calibration standards. Before you begin the calibration, check your cables' connectors under the stereo microscope and clean them. First, blow off debris with a short burst of canned air. Then use the lint-free swabs and isopropyl alcohol. Blow dry again with canned air.

Use the pin-depth gages to measure the pin depth and the dielectric depth of all SMA connections (i.e. on the analyzer, on the calibration standards, on your cables). If the cables are bad (i.e. the shoulder of the male pin extends beyond the mating plane - the plane of the outer cylinder around the dielectric), don't use them. Throw those cables away because they will damage the ECal and all the female 3.5mm cal standards in the lab.

Pretest the cables for phase stability. Attach safe cables - where "safe" means they've met the pin-depth and dielectric depth specs - to the test ports of the analyzer and tape down the ends of the cables. Attach a Short cal standard to the free end of the cable. Never rotate the cable or the cal standard. Rather, push them straight together and then finger tighten the nut. Then use the torque wrench and open-end wrench to tighten. Now verify that the LogMag trace for the cable is stable when you gently touch/jiggle the cables. Do this by plotting LogMag S11, then under the Display menu, hit Data $->$ Memory. Then change the display from "Data"to "Data Minus Memory". Immediately after storing into memory, you'll see the trace go down to -70 dB or so. Now gently wiggle the cable. If the trace stays under -30 dB, keep the cable - otherwise, throw it out. Joel Dunsmore won't use any cable that is worse than -40 dB (i.e. the trace goes higher than -40 dB) in this test. A second cable test is the SWR test. This time, attach a 50 ohm cal standard to the end of your cable. Under the Format menu, select SWR. If your cable was perfectly 50 ohms, and terminated by a perfect 50 ohm load, the standing wave ratio would be 1.00. If your cable with its connectors is lower than 1.20, it's fine. A third cable test is to display Phase S21 with your cable connected between Ports 1 and 2. Again, do Data $->$ Memory. Then display "Data Divided by Memory". This will zero out the Phase trace. Now gently wiggle the cable and see how much phase is left at the frequency of interest (for future labs, you'll be building amplifiers at ˜600 MHz). Measuring the parasitics of an 0603 component is equivalent to measuring about 1 degree of phase shift, so you want this phase instability error to be less than 1 degree.

Always remember to turn the display setting back to "Data" (don't leave it as "Data Minus Memory" or "Data Divided by Memory"). Note the upper left corner of the screen, where the info line is for the trace. The end of that line will say $[D - M]$ or $[D/M]$ if you've left those settings on.

Now do the entire calibration procedure. It's important, before calibrating, to look at the ECal or the mechanical cal standards you plan to use, under a microscope. Most importantly, check the female standards' inner receptacles' gold fingers. If any fingers are crushed, alert the GSI, because this means there is some bad cable in the lab which

was the culprit and we want to find it and throw it out before it wrecks other female cal standards.

Bring up the Calibration.ppt file on your laptop which has all the notes on calibration as you do this. This file is on the Lab Resources web page on the course website. When you calibrate, or during subsequent measurements, make sure your hands are not touching the cables.

After you calibrate, verify your cal is good. Do this by measuring something *else* besides the standards you calibrated with - some other cal standard that has a known model. Verify that its measurements match its model. The Calibration.ppt file shows what the traces should look like when things are working correctly.

Once you've verified you have a good cal, re-check the ECal or female mechanical standards under the microscope - to ensure you didn't crush any gold fingers. Then get checked off from the GSI. Now you can start this lab.

2. We'll use a Thru board to characterize the transmission lines. Solder end-launch SMA connectors onto the Thru board. You'll also need to solder end-launch connectors to your other 3 boards (Open, ShuntShort and ShuntDUT), so go ahead and do that. Actually, if you want to make life easier on yourself, mill or file down the boards so that they are all the same length (there is a jig on the GSI desk in the lab that lets you fit boards to it, in order to see that they're the same size. This is not strictly necessary, as you can also calculate the compensation times required for the different line lengths). Be aware though, that characterization of the parasitics of these 0603 components requires precise measurements. The gap across which an 0603 component is soldered onto a board, is only 700 microns, which is equivalent to a very small phase delay. If your cables aren't phase stable, you won't get this lab to work.

   When soldering the end-launch SMA connectors onto your boards, make sure to solder the backsides correctly A picture of the correct result is in Dr. Dunsmore's book in Chapter 9, and it's also shown in the SolderingPics.ppt file on the course website.

   We'll assume that the width of the transmission line traces are the same on all boards used for subsequent labs (and we assume that all boards are the same thickness). This is a fairly good assumption, as all the boards were probably fabricated together on a single panel, at the board house. Even though these transmission lines were designed to be 50 ohms, due to manufacturing tolerances, they probably aren't. FR4 is also a very lossy material, so these transmission lines need to be characterized by α in addition to Z_0 and β and ℓ. You'l want to create a per-unit-length model of this Thru board's transmission line so that you can later make accurate models for all transmission lines in Labs 2 and 3.

   Watch the 11/30/12 video in which Dr. Dunsmore describes how to do this measurement. He shows how to use the Fixture Simulator feature of the network analyzer to measure the characteristic impedance of this transmission line. Start by cutting off the center pin of an end-launch SMA connector. Then solder a small piece of copper sheeting or small piece of wire to short the center contact to the surrounding portion of the case. We'll call this device our "SMA-dummy-short". Attach this dummy short to the

end of the cable attached to Port 1. Use manual port extension, with loss, to move the reference plane to the end of that dummy short. You do this by displaying Phase S11 and then going to the Calibration menu (Cal hard key) and choosing Port Extension. Turn Port Extension on with the soft key. Type in some number of picoseconds until the phase is roughly flat at 180 degrees for all frequencies. You should find it requires around 36 ps or so. It will be helpful to be able to zoom in to a finer resolution of phase to accomplish this adjustment. On the Scale menu (Scale hard key), you can select the Phase Offset soft menu item and add 180 degrees of offset. Now you can zoom in and fine-adjust the Port Extension value until the phase is flat at 0 degrees for all frequencies. Now set the loss in the Port Extension menu. You'll need to display LogMag S11 to do this. You'll see that there is more return loss at higher frequencies. You want to make this trace flat at close to 0 dB for all frequencies. Note the return loss at two frequencies (use markers). Write down the slope of the attenuation per freq (since you know the length of this board, you can transfer this loss compensation to other boards later, on a per-unit-length basis). Then type those values into the Port Extension loss menu in order to flatten out the trace. Once you've done these steps, you've effectively moved the reference plane for zero phase and zero loss to the shorted plane of the dummy short.

Set the Phase Offset back to zero after you've finished setting Port 1's Port Extension.

Repeat for the Port 2 cable (i.e. take the dummy short off the Port 1 cable and attach it to the Port 2 cable, etc.). When finished, the network analyzer will have its new Port 2 reference planes set to the location of the dummy shorts' shorted plane.

Remove the dummy short from the Port 2 cable and attach the Thru board between the Port 1 and Port 2 cables. Effectively, you've moved the reference planes (plane of measurement for zero phase and zero loss) to the edges of your Thru board. Now measure a Thru board's S-parameters. Save the scattering parameters of this Thru structure. Name the output file "`thru_refedges.s2p`".

The Thru board's length, the distance between the end faces of the SMA connectors, is approximately 25 mm. Measure this distance between the two reference planes precisely with the lab's calipers. You'll use this length for the $d0$ in your transmission line model. With the Thru board attached, you can gain a number of insights about the transmission line, in real time on the VNA screen. First, display Phase S21. You can measure the electrical length - the time it takes a wave, of any frequency, to travel along this transmission line - of this Thru board in a manner analogous to what you just did to set the Port Extensions when you had the dummy shorts attached. However, we'll use Electrical Delay this time to measure the electrical length. The Electrical Delay feature applies to a single trace. In contrast, Port Extension applies to all traces for a given Port. You can find the Electrical Delay soft menu key under the Scale menu (Scale hard key). Type in various picosecond delays until the phase is flat at 0 degrees. You should get around 150 ps or so. The Thru boards in the lab are not cut to exactly the same length. Let's call this time, τ_0. You can calculate the velocity as $vel = \frac{d0}{\tau_0}$. The effective relative dielectric constant, ϵ_{re} of this microstrip transmission line can be backed out from the velocity. The velocity is related to the speed of light, c, and the

effective relative dielectric constant by: $vel = \frac{c}{\sqrt{\epsilon_{re}}}$. The effective relative dielectric constant of a microstrip is related to the bulk relative dielectric constant of the board material by several different author's models (e.g. [1] page 187, Eqn. 1.87 and [2] page 172, Eqn. 26 and [2] page 179, Eqns 33-34). The bulk relative dielectric constant, along with board geometry variables such as trace width and board thickness, is often used to calculate the line's characteristic impedance, Z_L (e.g. [2] page 165, Eqn 9) but we'll measure Z_L directly on the VNA.

Set the Electrical Delay back to zero after you've finished the electrical length measurement of this Thru board.

Next, you need to measure the characteristic impedance, Z_L, of this Thru's transmission line. To do this, display LogMag S11 in an upper window and an impedance Smith Chart in a lower window on the VNA. The reference impedance, Z_0 for the VNA itself for each port is 50 ohms. If the Thru's transmission line Z_L was a perfectly matched 50 ohms, then the VNA would measure an impedance, Z_m, of 50 ohms (i.e. a dot at the center of the Smith Chart and minus infinite dB's on the LogMag plot). However, your Thru board's Z_L is likely to be something other than 50 ohms, and so the measured Z_m is going to be something else again. Watch Joel Dunsmore's video from 11/30/12 or look at the `Lab1_addendum.ppt` file on the course website to see how you can use the VNA to figure out what Z_L is. Basically, the LogMag S11 traces will have bumps that peak at the frequency corresponding to lambda/4. Put a marker on that peak and look at the corresponding marker at that same frequency on the impedance Smith Chart. You can read off Z_m at the lambda/4 frequency from the Smith Chart. At the lambda/4 frequency, Z_L has been transformed to Z_m by: $Z_m = Z_L^2/Z_0$, so you can calc Z_L. You can then use the Fixture Simulator feature of the VNA to reset its reference impedance (if you change its reference impedance from 50 ohms to Z_L, your measured Z_m will appear as a dot at the center of the Smith Chart, and the return loss trace will flatten out). Remember to turn off the Fixture Simulator when you've finished with this experiment. That is, reset the VNA's reference impedance back to 50 ohms.

Now you've got all the parameters you need for a transmission line model. Most simulator tools such as ADS or MWO have tline elements that accept Z_L, ϵ_{re} and $d0$. When you simulate your Lab 2 or Lab 3 design later, you can use the lengths of the transmission lines on those boards in place of $d0$ in this model.

You can also use these tline characteristics to model the parasitics of an 0603 component in the manner outlined above in Section 4.3. The gap in the Open board for an 0603 component is 0.7 mm. A transmission line of 0.7 mm would be one way to model the parasitics of that gap (i.e. the parasitics of an 0603 component soldered across that gap). Calculate the component values for L and C that form a pi (CLC) model of a 0.7 mm length of this transmission line. In the next steps, we'll do some different measurements to get at these parasitic models another way. However, before we go to the next board, take one more measurement of this Thru: calculate for the dimensions of this Thru how to adjust the Port Extension delays so as to move the reference planes to within 0.7 mm of each other. It doesn't matter exactly where this 0.7 mm length is located along your transmission line, but you can set it so that one of the transmission

lines will have the same length as one of the transmission lines on the Open board. This will save you time in a subsequent step. Adjust the loss, as described below and analogously to what you did for the dummy short. The resulting VNA measurements are then representative of just a 0.7 mm length of this transmission line (i.e. the reference plane for zero phase and zero loss is the new Port Extension location for Port 1). Save this as measurement as "`Thru_0p7mm.s2p`". After this, set the Port Extension, and Loss parameters, back to what the were before you changed them (i.e put the reference planes back to the locations of the dummy shorts' shorting planes).

3. Solder end-launch SMA connectors to the Open board (Fig. 19a) if you haven't already done so. Use the calipers to measure the distance between the reference planes of the SMA connectors' faces. Also measure the gap, which should be 0.7 mm, and measure the lengths of the tlines to the left and right of the gap. Use the manual port extension feature to move the Port 1 and Port 2 reference planes to the edges of the Open's gap. Do this by assuming that the velocity of the Open board's tline will be the same as the velocity you measured on the Thru board, and by calculating how much time you'll need to add to each Port Extension in order move the reference planes to the location of the gap's edges. Also adjust the Loss settings in the Port Extension menu in a similar manner to what you did when you compensated the dummy-shorts. That is, assume the attenuation per GHz per mm will be the same on the Open board as it was on the Thru board. Once you've adjusted the Port Extension values for each of Port 1 and Port 2, you've essentially moved the reference planes for zero phase and zero loss to the edges of the Open's gap. Now any subsequent measurements of the Open board allow you to"see" the gap's S-parameters by themselves without the distraction of characteristics of the transmission lines getting mixed into the measurements. Watch Joel Dunsmore's video from 11/30/12, as he teaches all the insights one can see from looking at the S21 magnitude and phase (e.g. characterizing the parasitic extrinsic capacitance across the gap, which will always be there whenever you solder a component to the board). Save this measurement as `Open.s2p`.

4. Measure and save the scattering parameters of the ShuntShort board ('shuntshort.s2p'). Since this structure is symmetric, you only need to measure it as a 1-port, but you should measure it as a 2-port in order to see the non-ideal transmission properties. You'll note that the ShuntShort does not perfectly reflect the incoming signal. In fact, at high frequencies, a large percentage of the Port 1 transmitted wave makes its way to Port 2. This ShortShunt measurement can be used to estimate the parasitics of a component soldered to ground (as it includes the via to ground parasitic inductance).

5. Next, measure the two-port S-parameters of a zero ohm resistor connected in series (Fig. 20a) and name the file 'zero_ohm_series.s2p'. Note that an ideal zero ohm resistor would produce no reflection ($S_{11} = S_{22} = 0$, or minus infinite dB's) and perfect transmission ($S_{12} = S_{21} = 1$, or 0 dB). Any deviation from this ideal performance can be attributed to the parasitics of this component. Save the S2P file for this measurement.

6. Now measure the two-port S-parameters of a zero ohm resistor to ground soldered in shunt ('zero_ohm_shunt.s2p'), as shown in Fig. 20b. Only solder one component to

ground (it's possible to fit up to two components on the board). Note that an ideal zero ohm resistor to ground would produce a perfect reflection ($S_{11} = S_{22} = 1$, or 0 dB) and zero transmission ($S_{12} = S_{21} = 0$, or minus infinite dB's). Any deviation from this ideal performance can be attributed to the parasitics of this component. Save the S2P file for this measurement.

7. To avoid wasting a board (and to match the port extension)[4], de-solder the zero ohm resistor and replace it with an inductor with $L < 10$ nH. Measure the inductor in series and shunt. Save both S2P files as 'ind_series.s2p' and 'ind_shunt.s2p'.

8. Using the network analyzer, measure the magnitude and phase response of the *impedance* of the 1-port structure (component soldered to ground). VNAs measure S-parameters, but the Equation Editor on the Display menu (hit the Display hard key) lets you change the active trace (the trace that is highlighted) to display the result of an equation. The Equation Editor lets you choose, as variables, the various S-parameters and also the x-axis frequencies. You can then write an equation for the input impedance as a reflection conversion equation See Dunsmore's book, p. 118, Eqn. 2.26: $Z_{refl} = Z_0 \frac{(1+S_{11})}{(1-S_{11})}$. Then you can set the Format menu to display LogMag Z_{refl} and Phase Z_{refl}. If you set the x-axis of the LogMag plot to be a log sweep (hit the Sweep Setup hard key), then the trace will look like a Bode plot. It will be flat at low frequencies below the RL breakpoint frequency, and then a positive 20 dB/decade slope of an inductance above the breakpoint frequency. Estimate the inductance and resistance directly, using markers. Placing a marker at low frequency allows you to read off the resistance directly. Note that you can allocate another trace and make an equation for it for effective inductance by dividing Z_{refl} by omega. Placing a marker on that trace, above the breakpoint frequency, enables you to read off the inductance directly. Replace with the ShuntShort board, and estimate the resistance and inductance of the ShuntShort directly also.

9. Repeat the last two steps with a capacitor component with $C < 10$ pF. To avoid wasting a board (and to match the port extension), re-use the same board by de-soldering the inductor. Name the files 'cap_series.s2p' and 'cap_shunt.s2p'.

10. Using the highest frequency VNA in the lab, measure this capacitor up to 8.5 GHz. Name the file 'cap_series_hf.s2p' and 'cap_shunt_hf.s2p'.

8 Post Laboratory

1. Using the measurements on the "`Thru_0p7mm`" structure, calculate the equivalent circuit for the short section of transmission line. You can do this by converting the S parameters to Y parameters and then forming a Π circuit. (Note: I never was able to get this to work correctly. At 600 MHz, the L and C values always came out negative. Perhaps the measurement is too precise to make. Maybe moving the reference planes for zero phase and zero loss is not enough. I've tried everything except the

[4]SMT components are very inexpensive (cents) whereas low volume custom PCBs are expensive!

time-gating as in Dunsmore Chapter 9, which also removes mismatches.) You can refine this model by matching the measured S parameters to the model results (use the tuning or optimizer features in ADS or MWO).

2. Compare the component values of the equivalent circuit to calculated component values based on transmission line theory.

3. Repeat the above steps for the "short to ground", zero-ohm shunt and series components. Estimate the extra inductance due to the via structure.

4. Compare the measurements and models of the zero-ohm structures to the short structures. Explain any differences or similarities. Generate S-parameter plots (mag/phase/Smith) of measurements versus model. Note that Smith plots are only relevant for reflection measurements, S_{11} or S_{22}.

5. Use the above steps to create models for the capacitor and inductor components. Generate S-parameter plots (mag/phase/Smith) to compare the measurements to the modeled components.

6. Create models of the shunt/series inductor/capacitor directly from measurements from the zero-ohm resistor structures by using the manufactured component value and the extrinsic parasitics. How close is the *a priori* model compared to the *a posteriori* model? This is an important step since it avoids creating custom models for every component. Compare the results qualitatively and quantitatively using plots of S-parameters (mag/phase/Smith).

7. Using the high-frequency measurements, compare the model to measurement results. Up to what frequency do you trust your model? Plot S-parameters (mag/phase/Smith).

8. Your final lab write up (PDF format) should be easy to read and summarize all of your pre-lab and post-lab results. Please do not paste several plots together and expect us to understand the order and logic behind your results. Include a coherent write-up, clearly drawn or computer generated schematics of your models and plot comparisons between model and measurements. Include all the measured S-parameters (mag/phase/and Smith Chart format) and compress the file and upload it to the class submission site (use ZIP or a gzip'ed tar ball).

9. How much time did you spend on this lab? Any feedback is appreciated.

9 References

Check online for sites that discuss SMT, PCB manufacturing, Network Analyzers, for instance in the *RFCafe* website. Another good source is Wikipedia, search the terms 'capacitor', 'inductor', and 'surface mount technology'. Documentation on the network analyzer is available in the lab and on the class website. Also refer to Agilent's online documentation. Two very useful books are:

[1] J. Dunsmore, "Handbook of Microwave Component Measurements," Wiley, 2012. One copy is kept in the lab and it's also available as an e-book at the UCB library site.

[2] T. Lee, "Planar Microwave Engineering," Cambridge Univ. Press, 2004. Available in hard copy at the library.